THE UNIVERSITY OF DANANG
UNIVERSITY OF SCIENCE AND TECHNOLOGY
FACULTY OF ELECTRICITY

CAPSTONE PROJECT

MAJOR: CONTROL ENGINEERING AND AUTOMATION

CAPSTONE:

DESIGN OF A DUTY CYCLE DETECTOR FOR HIGH-SPEED INPUT SYSTEM

Supervisor:	**Dr. NGUYEN KHANH QUANG**
Co-supervisors:	**Eng. THAI HOANG HUNG**
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Class:	**20TDHCLC1**

Da Nang, 06/2025

SUMMARY

Capstone: **DESIGN OF A DUTY CYCLE DETECTOR FOR HIGH SPEED INPUT SYSTEM (DCD)**

Conducted by:

1) Huynh Van Hong Sang – Student ID:105200380- Class: 20TDHCLC1

In the context of the continuous advancement of semiconductor and integrated circuit technologies, modern electronic systems increasingly demand higher processing and data transmission speeds. Data transmission protocols such as DDR. (Double Data Rate), USB (Universal Serial Bus), have become critical standards across various high-tech devices

In parallel, artificial intelligence, especially deep learning, requires large input datasets for training and inference, placing high demands on signal processing and transmission speed. In such high-speed systems, precise control of the signal's duty cycle (DC) is crucial, as it directly impacts the reliability and efficiency of data transmission. As circuit speeds increase, phenomena such as DC distortion, offset, and jitter become more prominent, potentially leading to transmission errors, signal degradation, data loss, or reduced system performance.

Therefore, researching and developing an effective DC detection method is essential to improve duty cycle accuracy in high-speed systems. A reliable DC detection solution not only minimizes signal deviation but also ensures the stable operation of key I/O protocols such as DDR., USB, even under varying PVT conditions (Process, Voltage, Temperature). Furthermore, such a method can be widely applied across a range of modern electronic systems—from mobile devices and personal computers to data centres, embedded systems, and telecommunications

In summary, amid the growing challenges of high-speed systems, the research, design, and implementation of an effective DC detection solution is not only theoretically significant but also of great practical value.

CAPSTONE PROJECT ASSIGNMENT

Num	Student Name	Student ID	Class	Majority
1	Huynh Van Hong Sang	105200380	20TDHCLC1	Control Engineering and Automation

1. *Capstone Project:*

   Design Of A Duty Cycle Detector For High-Speed Input System

2. *Project classification:* ☐ *Subject to an intellectual property agreement regarding the project outcomes*
3. *Contents of the explanation and design sections:*

Num	Student Name	Content
1	Huynh Van Hong Sang	Studied Linux commands, HSPICE simulation, Custom Compiler Design software, and Synopsys tools Researched CMOS, FinFET, fundamental effects in physical design, and techniques used in physical analog layout DCD researching Floorplan for layout part and routed signal paths for whole circuit Implement and check layout part results Collect DCOP data for Post-layout Simulation Write thesis document report and prepare slides for presentation

- Supervisor:

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Supervisor's full name Eng. Thai Hoang Hung	*Section / Content:* Guiding for layout techniques and related constraints

4. *Capstone Assignment Date: 23/03/2025*
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Da Nang, June 23rd, 2025

Head of Automation Department	**Supervisor**
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PROGRESS MONITORING FORM FOR GRADUATION THESIS PROJECT

(Form for advisors/student)

Student name: Huynh Van Hong Sang Student ID: 105200380

Thesis Title: Design Of A Duty Cycle Detector For High-Speed Input System

Advisor's name: Nguyen Khanh Quang Department: Faculty of electrical, Danang University of Technology

Week	**Date**	**Workload**		**Advisor's signature**
		Completed	**To be continued (%)**	
1	17/2/2025	5%	95%	
2	24/2/2025	7%	93%	
3	3/3/2025	10%	90%	
4	10/3/2025	**First review: Evaluation of completed workload: _____ %** ☐ Allowed to continue the thesis ☐ Not allowed to continue the thesis		
5	17/3/2025	20%	80%	
6	24/3/2025	30%	70%	
7	31/3/2025	50%	50%	
8	7/4/2025	**Second review: Evaluation of completed workload: _____ %** ☐ Allowed to continue the thesis ☐ Not allowed to continue the thesis		
9	14/4/2025	70%	30%	
10	21/4/2025	75%	25%	
11	28/4/2025	85%	15%	
12	5/5/2025	**Third review: Evaluation of completed workload: _____ %** ☐ Allowed to continue the thesis ☐ Not allowed to continue the thesis		
13	12/5/2025	90%	10%	
14	19/5/2025	95%	5%	
15	26/5/2025	100%	0%	

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This thesis was written in the year 2025 under the supervision of Dr. Nguyen Khanh Quang, Faculty of Electricity, Danang University of Science and Technology, Mr. Thai Hoang Hung, A&MS Layout Senior Supervisor, Synopsys Vietnam Limited Liability Company in Danang, and Mr. Le Minh, A&MS Circuit Senior Engineer, Synopsys Vietnam Limited Liability Company in Danang.

First and foremost, we would like to express our sincere gratitude and deep regards to our supervisors Dr. Nguyen Khanh Quang, Mr. Thai Hoang Hung, and Mr. Le Minh for their patience, enthusiasm, immense knowledge, exemplary guidance, and constant encouragement throughout the period we work on this thesis.

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Danang, June 2025

Synopsys Danang

Huynh Van Hong Sang

DECLARATION OF AUTHORSHIP

I hereby declare that the thesis titled **"Design of a Duty Cycle Detector for high-speed input system"** is the result of my own work, carried out under the supervision of Dr. Nguyen Khanh Quang from faculty of electricity, Danang University of Science and Technology; Mr. Thai Hoang Hung, A&MS Layout Senior Supervisor, Synopsys Vietnam Limited Liability Company in Danang, and Mr. Le Minh, A&MS Circuit Senior Engineer, Synopsys Vietnam Limited Liability Company in Danang.

The content and results presented in this thesis are the outcome of my own research conducted during our academic studies at the university as well as our internship and project implementation at the company, All data, images, and information presented in this thesis are truthful, based on my own research and references from various sources, including documents provided by the company.

All data and results reported herein are truthful and accurate to the best of our knowledge. We take full responsibility for any issues that may arise and are fully aware of the disciplinary actions stipulated by the department and the university.

Student Author

Huynh Van Hong Sang

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ABBREVIATION

DDR	Double Data Rate
USB	Universal Serial Bus
DC	Duty Cycle
RAM	Random Access Memory
DCD	Duty Cycle Detector
DCA	Duty Cycle Adjuster
DCC	Duty Cycle Corrector
PVT	Process, Voltage, Temperature
CMOS	Complementary Metal Oxide semiconductor
LPE	Layout Parasitic Extraction
I/O	Input Output
LVS	Layout Versus Schematic
DRC	Design Rules Check
DRM	Design Rules Manual
ICV	Integrated Circuit Validator
EM	Electromigration
SR	Set Reset
FinFet	Fin Field-Effect transistor
MOM	Metal Oxide Metal
DCOP	DC operating point
AC	Alternating Current
SDL	Schematic driven layout

INTRODUCTION

1. Motivation

In high-speed electronic systems—particularly in communication standards such as DDR, USB, and PCI—ensuring a precise and stable duty cycle is a critical factor that directly impacts the system's performance and reliability. A significant deviation from the ideal 50% duty cycle can lead to functional errors, data loss, and considerable performance degradation. To address this issue, numerous duty cycle correction circuits have been studied and developed.

In designs operating at very high frequencies, semiconductor components such as transistors, logic gates, and signal transmission paths are subject to stringent timing constraints, which often result in signal distortion and attenuation. Furthermore, process, voltage, and temperature (PVT) variations exacerbate the challenge of maintaining consistent circuit behavior. With the adoption of advanced semiconductor technologies below 28nm, the effects of PVT variations become increasingly unpredictable, requiring more precise duty cycle detection and correction techniques.

Therefore, the research and development of an efficient duty cycle detection method is essential to enhance signal accuracy in high-speed systems. A reliable duty cycle detector not only minimizes signal deviation but also ensures the stable operation of critical I/O protocols such as DDR, USB under dynamic PVT conditions. Additionally, such methods can be widely applied across modern electronic domains, including mobile devices, personal computers, data centers, embedded systems, and telecommunications, contributing significantly to overall system performance.

In conclusion, in the face of mounting challenges in high-speed electronics, the design and implementation of an accurate and robust duty cycle detection solution is of both theoretical significance and practical value, strengthening system integrity, optimizing data transfer efficiency, and meeting the increasingly stringent demands of today's semiconductor industry.

2. Contribution of the thesis

Complete the circuit design for the Duty Cycle Detector including Bias Current and Folded Cascode to CMOS technology under the process node of 12nm with the design requirements of verification plan (DC, AC, Transient, Power) and simulation

with 35 cases of 3 corners TT, SS, FF with temperature -40, 25, and 125 Celsius degree and voltage supply is 0.765V, 0.85V, and 0.935V respectively.

Complete the layout design using layout analog techniques to avoid the non-ideal factors affecting the design when being under fabrication.

Extracting LPE netlist from layout for post-layout simulation and making result comparison between pre-layout and post-layout.

3. Organization of the thesis

There are four chapters in our thesis

Chapter 1: Overview of the Duty Cycle Detector for High-speed input system

Chapter 2: Literature Review on CMOS Technology

Chapter 3: Proposed Design for the High-Speed Duty Cycle Detector

Chapter 4: Experimental Results and Evaluation of the High-Speed Duty Cycle Detector

CHAPTER 1: OVERVIEW OF DUTY CYCLE DETECTOR FOR HIGH-SPEED INPUT SYSTEM

This chapter outlines the physical design and conceptual basis for implementing a Duty Cycle Detector (DCD) for high-speed input systems. Section 1.1 introduces the DCD's function and relevance. A preliminary solution is proposed in Section 1.2, with a breakdown of key sub-blocks (RC Low Pass Filter, Reference Voltage, Comparator, RS Trigger) in Section 1.2.1. Section 1.3 covers the layout design flow from schematic to physical design. Section 1.4 discusses expected outcomes such as power efficiency and area optimization. Section 1.5 presents evaluation methods to ensure design robustness across PVT variations. This chapter serves as the foundation for the thesis.

1.1 Overview

As high – speed circuits and systems operating with high frequency (depending in almost characteristic of clock signal which possible to be impacted by many unexpected factors) escalate year by year, duty cycle of clock must be precisely at 50%. A 50% duty cycle implies that pulse width of signal exactly half of period. It may call symmetric duty cycle or balance duty cycle. It ensures that signal spends band width for high state coincide with low state. This value of clock duty-cycle (DC) plays a vital role in getting the desired output. Furthermore, a 50% DC clock allows all the outputs to transform to coincide each of them for the sake of reducing delay time. It is a huge trouble if DC does not meet 50% specification because of the functional error impacting on data loss. However, the duty cycle will not be exactly 50% due to process variability, device mismatches of the clock driver to a lot of cells led to the certain amount of duty cycle error providing a low performance.

The clock signal is defined by some parameters such as frequency, period, and duty cycle. Duty cycle is the key in high speed I/O circuit analysis which fundamentally relies on ratios of pulse width (PW) on time and period of signal components. The formula to calculate the DC is:

$$DC = \left(\frac{\text{Pulse width}}{\text{Period}}\right) \times 100 \quad (1.1)$$

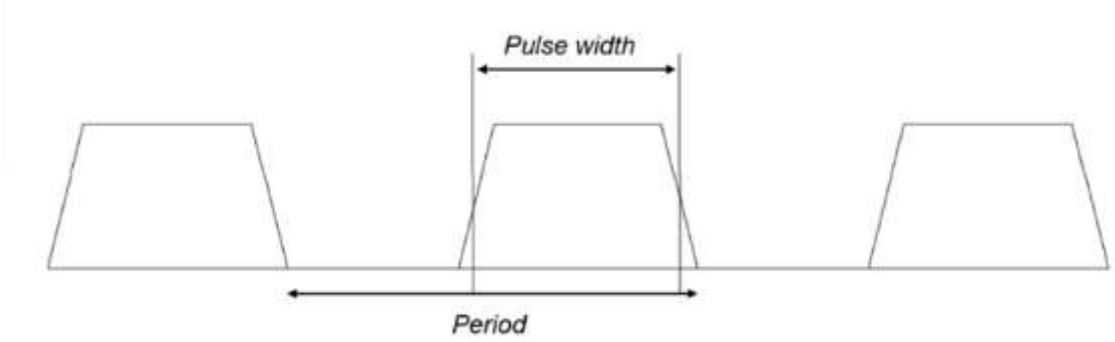


Figure 1.1 Duty Cycle

In recent years, the human's requirements are more challenging when they want to transfer and receive more data faster. In this case, Double Data Rate Synchronous Dynamic Random-Access Memory (DDR SDRAM) is proposed which able to transfers data at both rising and falling edge instead Single Data Rate (SDR SDRAM), which allowed to transfers data at only raising or falling edge so that data contain in the haft of period instead of a full period of clock so that timing requirement is regard to DDR.

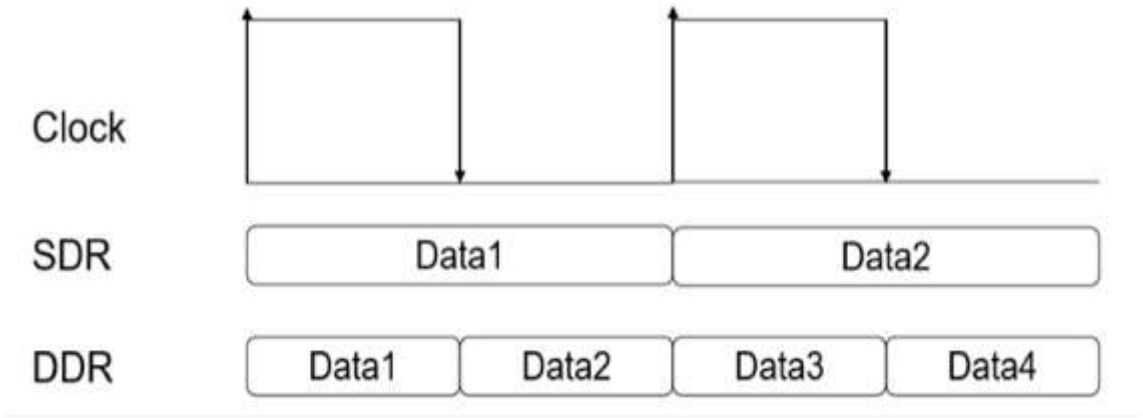


Figure 1.2 Comparing DDR and SDR

To deal with this problem, Duty Cycle Corrector (DCC) is proposed to make the DC as close as 50%. DCC consist of 2 main blocks:

- Duty cycle adjuster (DCA).
- Duty cycle detector (DCD).

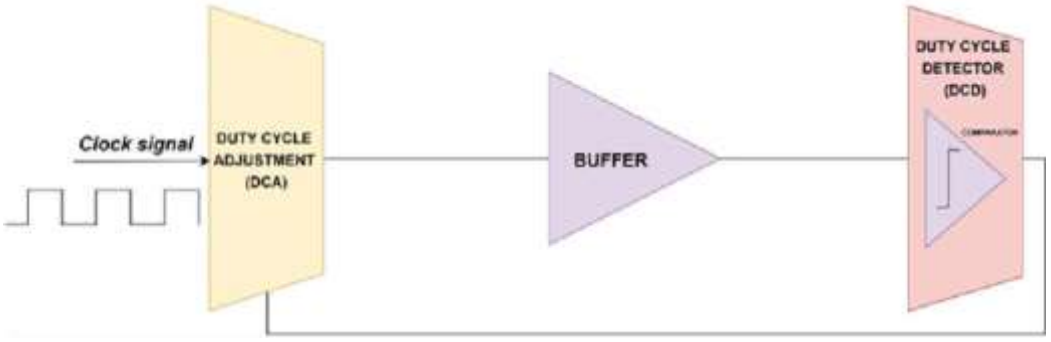


Figure 1.3 Block diagram of DCC

DCA manipulates for getting desired DC then sends it to DCD. The duty cycle detector measures correctly DC error (%) to make a right decision to end operation or send a signal to DCA to request a new cycle of operation. If DCD sends "0", DCA will adjust to increase orientation, in contract, if the signal "1" is sent to DCA, it will adjust to decrease orientation. Hence, to get a justifiable performance in the system, reliable architecture must be designed for DCD.

1.2 Preliminary solution

Our proposed DCD circuit is an analog-mixed-signal with the input clock frequency is 8GHz using 12nm FinFET technology.

DCD function is a correct measure of the DC error (%), make a right decision to send it to output. Value of DC detector output is 0 if duty cycle is less than 50 percent and vice versa, the output is 1 if it is greater than 50 percent. The architecture of DCD is shown in this figure below:

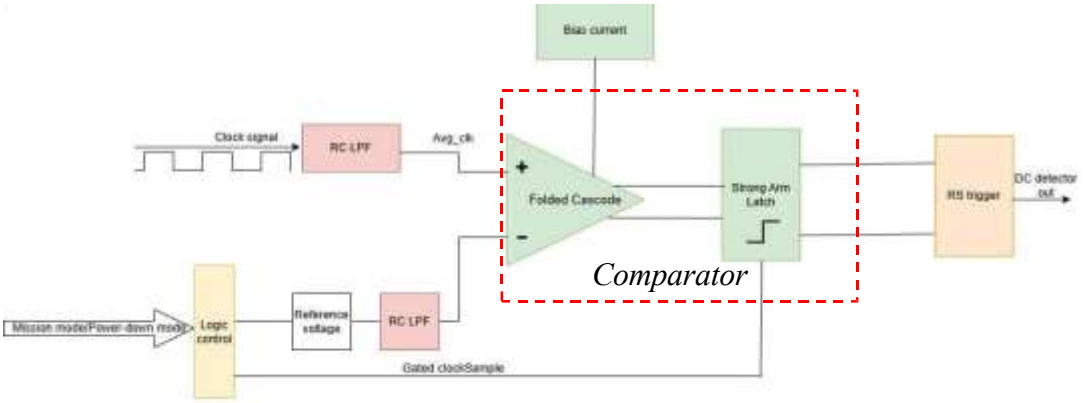


Figure 1.4 DCD Block Diagram

Duty Cycle Detector mode is config DCD into two different functional modes: mission mode and power-down mode.

- Mission mode: Compare two input voltage level and output to logic “1” or “0” at DC detector out.
- Power-down mode: When the circuit is not in use, it is disconnected or disabled to save power consumption.

In this thesis, we focus on the mission mode and power-down mode of DCD circuit.

1.2.1 The detailed sub-block of Duty Cycle Detector

The analog DC detector core contains:

1.2.1.1 Bias Current

One effective technique is the use of a threshold voltage-referenced biasing circuit.

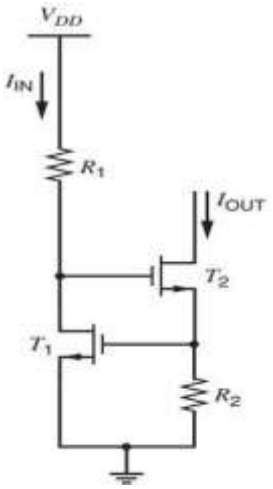


Figure 1.5 Structure of Threshold Voltage-Referenced Bias Circuit

The threshold voltage-referenced biasing circuit exploits the physical characteristics of MOS transistors operating in the low-current region—that is, in the weak or moderate inversion region. In this region, the gate–source voltage (V_{GSn}) of the transistor is typically close to its threshold voltage (V_{tn}), and the overdrive voltage ($V_{GSn} - V_{tn}$) is small. This enables the generation of a stable bias current that depends primarily on VTand a well-defined resistor, rather than linearly on the supply voltage VDD.

The basic structure of a threshold voltage-referenced bias circuit usually consists of a MOS transistor (typically denoted as M_1) and a resistor (R_2).

The transistor M_1 is biased by a small current I_{bias} to establish a suitable V_{GSM}. This gate-source voltage is then used to generate an output current I_{OUT} by placing resistor R_2 in series with one of the circuit's nodes, resulting in the relationship:

$$I_{OUT} = \frac{V_{GSM1}}{R_2} = \frac{V_{TN} + V_{OV1}}{R_2} = \frac{V_{TN} + \sqrt{\frac{2I_{bias}}{\mu_n C_{ox}(W/L)_1}}}{R_2} \quad (1.2)$$

Under ideal conditions, when I_{IN} is small and the W/L ratio of transistor M_1 is sufficiently large, M_1 operates in the region where V_{GSM} is approximately equal to V_{TN}. In this case, the output current I_{OUT} is also approximately equal to V_{TN} divided by R_2.

Thus, I_{OUT} is no longer directly dependent on the supply voltage (VDD), but instead primarily depends on two quantities:

- the threshold voltage V_{TN}, a technology-dependent parameter, and
- the resistor R_2, which can be accurately designed.

A clear advantage of this biasing circuit is its ability to significantly reduce the sensitivity of the bias current to variations in the supply voltage.

Since the output current I_{OUT} is determined by the threshold voltage V_{TN} and a resistor, fluctuations in VDD have only an indirect—and very limited—impact on I_{OUT}.

This feature is especially important in applications that require high stability and must operate over a wide supply voltage range.

The sensitivity of the bias current to VDD (defined as the relative derivative of I_{OUT} with respect to VDD) is generally much lower than that of circuits using direct resistor-based biasing.

1.2.1.2 RC Low Pass Filter

RC Low Pass Filter is used to convert high speed clock signal into DC signal which is able to compare with another DC signal (reference DC signal).

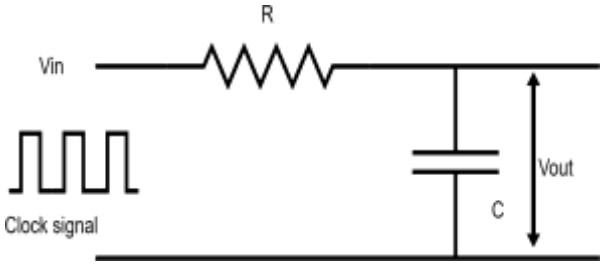


Figure 1.6 Simple RC Low Pass Filter

1.2.1.3 Reference Voltage

Reference voltage is used to generate reference DC signal which is able to compare with DCD signal. Conventional topology use a resistive voltage divider.

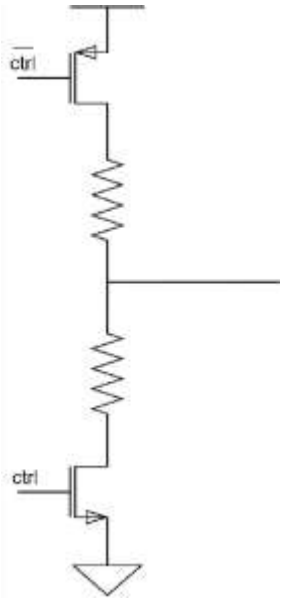


Figure 1.7 Voltage Divider

1.2.1.4 Comparator

Comparator is an electronic circuit, which compares the two inputs that are applied to it and produces an output. The output value of the comparator indicates which of the inputs is greater or lesser.

The comparator circuit consists of two main blocks: the Folded Cascode amplifier and the StrongARM latch, which together form the most critical component of the Duty Cycle Detector.

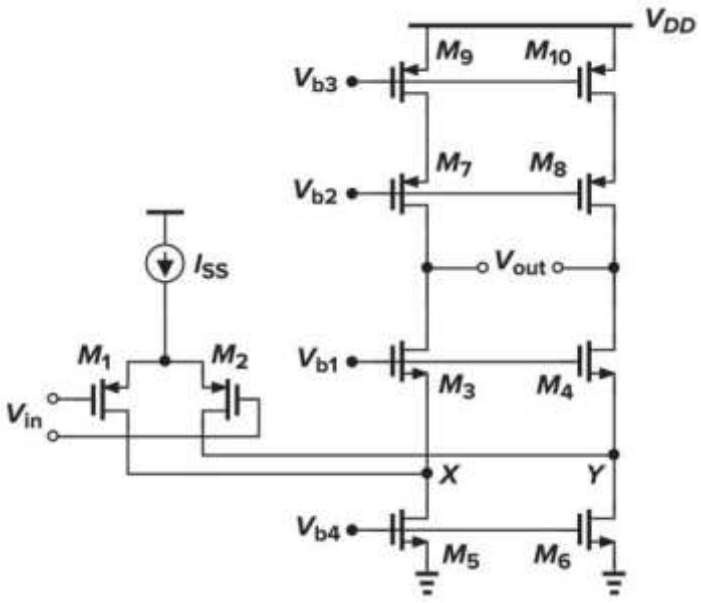


Figure 1.8 Schematic diagram of folded cascode differential amplifier

The folded cascode differential amplifier is designed to achieve high voltage gain and to improve common-mode performance. In this architecture, the signal current is "folded" through different types of transistors, optimizing the overall operation of the circuit.

Some advantages of the folded cascode design include:

- Greater flexibility in selecting common-mode voltage levels for both input and output stages.
- Lower supply voltage requirements compared to the telescopic cascode architecture.
- Higher voltage gain when using NMOS input transistors, due to the higher electron mobility compared to holes in PMOS devices.

These characteristics make the folded cascode amplifier an ideal choice for applications that require high performance and excellent stability.

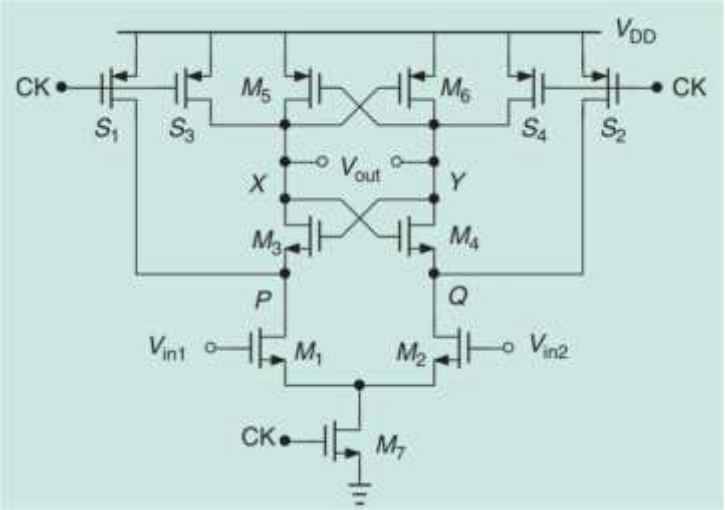


Figure 1.9 Schematic diagram of Dynamic Strong-arm Latch

After amplifying the voltage difference between the two input signals, it is necessary to convert that difference into a digital value of logic “1” or “0”. At this stage, a Dynamic Comparator based on the StrongARM Latch architecture is employed.

In terms of structure, the StrongARM latch circuit consists of an input transistor pair M1–M2 controlled by a clock signal, two cross-coupled pairs of NMOS (M3–M4) and PMOS (M5–M6) transistors, and a set of precharge switches (S1–S4) for initializing the circuit. The differential pair M1–M2 serves to amplify the voltage difference between the inputs Vin1 and Vin2. The cross-coupled transistor pairs establish positive feedback during the comparison phase, driving the output towards one of the logic states. The structure is illustrated in the figure 1.9

Each transistor in the circuit plays a distinct role:

- M1–M2: Input differential pair, responsible for signal amplification.
- M3–M4: Disconnect the DC current path after latching, ensuring zero static power consumption.
- M5–M6: Reinforce the output back to high logic level during regeneration.
- M7: Tail current source, activated by the clock signal.
- S1–S4: Precharge switches to reset critical nodes before evaluation.

1.2.1.5 RS trigger

The RS Trigger Circuit, also known as the RS (Set-Reset) flip-flop, is one of the most fundamental memory elements in digital circuits. Its simple structure consists of two cross-coupled NAND gates (or NOR gates in alternative versions), where the output

of each gate is fed back to the input of the other. The two control inputs are labeled S (Set) and R (Reset), which allow the circuit to store or change its output state depending on the input signal combinations.

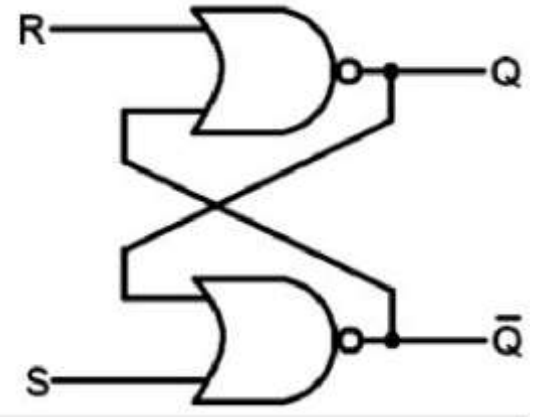


Figure 1.10 RS Trigger

During operation:

- When S is high (1) and R is low (0), the output Q is set to 1 and the inverted output kş[becomes 0 – this is referred to as the "set" state.
- Conversely, when R = 1 and S = 0, the circuit enters the "reset" state with kş = 0 and kş[= 1.
- If both inputs are high (1), the circuit maintains its previous state, demonstrating its ability to store one bit of information.
- However, when both inputs are low (0), the circuit enters an undefined state, which is prohibited in practical applications.

1.3 Layout Design Flow:

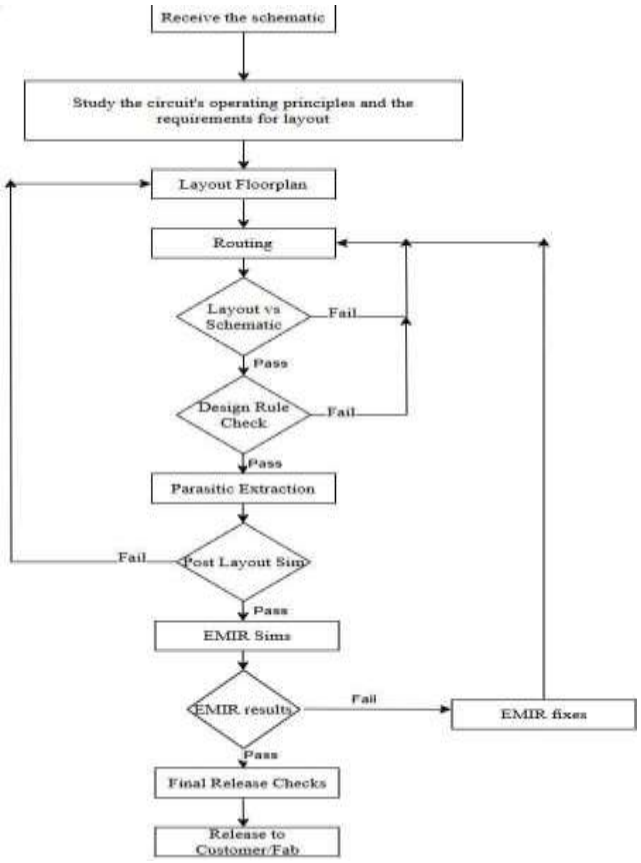


Figure 1.11 Layout Design Flow

1.4 Expected Results:

In this thesis, the layout design of the Duty Cycle Detector (DCD) is presented. The DCD circuit, incorporating both the bias current source and folded cascode amplifier, is implemented using advanced 12nm FinFET technology. The design operates under supply voltages of 0.765 V, 0.85 V, and 0.935 V, with temperature variations ranging from -40°C to 125°C. After post-layout simulation, the DCD circuit is required to meet the performance specifications outlined in Table 1.1.

Table 1.1 DCD Specification

Parameter	Specification		Unit
	Min	Max	
Supply voltage	0.765	0.935	V
DC Gain	16	-	dB
Gain Margin	20	-	dB
Phase Margin	50	-	Degree
Vcm in mission mode	250	-	mV

1.5 Evaluation method:

The circuit will be evaluated based on the following methods:

DC Operating Point: Used to determine the operating region of MOSFETs and extract key values such as drain current (I_D), gate-source voltage (V_{GS}), drain-source voltage (V_{DS}), and threshold voltage (V_{TH}).

Transient Analysis: Performed to analyse the circuit's time-domain response over a defined interval in order to measure parameters such as average values, V_{CM} (Common mode voltage) and power consumption in mission mode and power-down mode.

Design Rule Checking (DRC): Ensures that the layout complies with the foundry's design rules, including constraints on minimum feature size, line width, and spacing between components.

Layout versus Schematic (LVS): A verification step that compares the physical layout with the original schematic to ensure that all devices and interconnections are correctly implemented and functionally matched.

1.6 Chapter Conclusion:

Chapter 1 has provided an overview of the necessity of designing a duty cycle detector for high-speed input systems, especially under the challenges posed by advanced semiconductor scaling and PVT variations. The chapter also reviewed relevant prior studies, introduced a preliminary solution which includes function of each block, presented the physical layout design flow, defined the expected output parameters, and outlined the evaluation methods.

These foundations set the stage for the detailed design and implementation steps presented in the following chapters.

CHAPTER 2: LITERATURE REVIEW ON CMOS TECHNOLOGY

In this chapter, the CMOS theory is considered in several listed aspects: the most important concepts: Basic knowledge about MOSFET transistor devices including NMOS and PMOS, which could be listed as: structure, operation region, drain current, and parasitic capacitance. Basic knowledge about the second-order effects such as body effect, channel-length modulation, and subthreshold conduction. Basic analog circuits used in this project: Current mirror. And also theories and technique relating to analog layout

2.1 Basic CMOS theory

2.1.1 Structure of NMOS

MOSFET, which stands for Metal-Oxide Semiconductor Field-Effect Transistor, is a type of Field-Effect transistor. It is fabricated on a p-type or n-type substrate called the “bulk” or “body”. In the figure 2.1 below, NMOS (n-type) device is fabricated on p-type substrate. The devices consist of 4 terminals: Gate (G), Source (S), Drain (D), and Body/Bulk (B). The two terminals Source and Drain are heavily doped n regions, the Body terminal is heavily doped p region. Polysilicon or “poly” operates as a Gate and a thin layer of silicon dioxide (□□□□) insulates the Gate from the substrate.

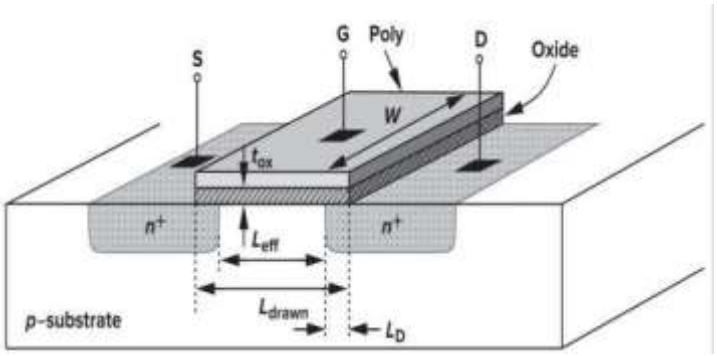


Figure 2.1 Mosfet Structure

2.1.2 Operation regions, Derivation of I-V Characteristic

A NMOS device has simply three terminal Gate (G), Drain (S), Source (S). Based on the voltage applied to each terminal, it has 3 working operations.

When □□□□ < □□□: transistor works in cut-off region, it does not conduct current. When the gate-source voltage is less than the threshold voltage the channel is not former between the source and drain of the device is not formed hence it cannot conduct the drain current.

When $V_{GS} > V_{Th}$ & $V_{DS} < V_{GS} - V_{Th}$: it works in triode region and conduct a current from drain to source called drain current. As the gate-source voltage applied to G and S terminal of NMOS is higher than the threshold voltage, the inversion layer between the Source and Drain increases, leading to more electrons moving to this region. When the voltage is applied to the Drain terminal, it pulls the electrons from the Source to the Drain hence there is a current flowing from the Drain to the Source of transistor called the Drain current. The Drain current increase a as parabolic function:

$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{Th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (2.1)$$

When $V_{GS} > V_{Th}$ & $V_{DS} \geq V_{GS} - V_{Th}$ **:** transistor turns into saturation region when the pinch-off phenomenon happens. Ideally, the drain current will remain constant if channel length modulation effect is neglected. Otherwise, it increases linearly depending on the increase of V_{DS}. We have formula for I_D in this region without and with considering of channel length modulation effect respectively.

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2 \quad (2.2)$$

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2 (1 + \lambda V_{DS}) \quad (2.3)$$

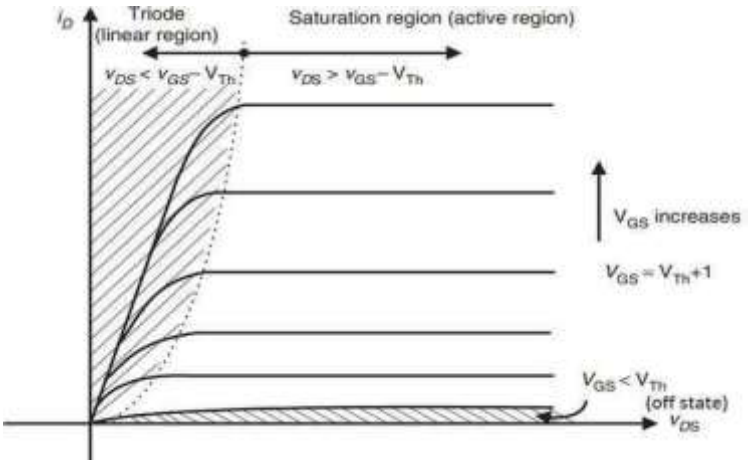


Figure 2.2 I-V curve and working regions of NMOS

Figure 2.2 illustrate the full I-V curve of NMOS with its conditions and working regions. Here the channel-length modulation is negligible.

2.1.3 Secondary effect:

In this thesis, we will analyze the secondary effects of MOSFET which include 3 important effects: the body effect, channel length modulation and sub-threshold

conduction. These secondary effects can be negligible in digital circuit designs, but they have a significant impact on analog circuits

2.1.3.1 Body effect:

Thus far, it has been assumed that the source-bulk voltage $^{a}c_{m\dagger}$ is zero. With $^{a}c_{m\dagger} = 0$, the MOSFET behaves as if it were a three-terminal device. However, we find many circuits, particularly in ICs, in which the bulk and source of the MOSFET must be connected to different voltages so that $^{a}c_{m\dagger} \neq 0$.

When $^{a}c_{m\dagger} > 0$, the depletion width of the p-n junction between the source and the substrate increases, which makes it more difficult to create a channel with the same $\mathfrak{r}_{\dagger hm}$ and effectively reduce the channel depth. Body effect has a great impact on threshold voltage and can be modeled by

$$\mathfrak{r}_{nd} = \mathfrak{r}_{nf} + \gamma(\sqrt{\mathfrak{r}_{m\dagger} + 2\Phi_{\mathfrak{z}}} - \sqrt{2\Phi_{\mathfrak{z}}}) \qquad (2.4)$$

where $\mathfrak{r}_{nf}$: zero-substrate-bias value for $\mathfrak{r}_{nd}$ (V)

χb : body-effect parameter ($\sqrt{\mathfrak{r}}$)

$2\emptyset_{\mathfrak{z}}$: surface potential parameter (V)

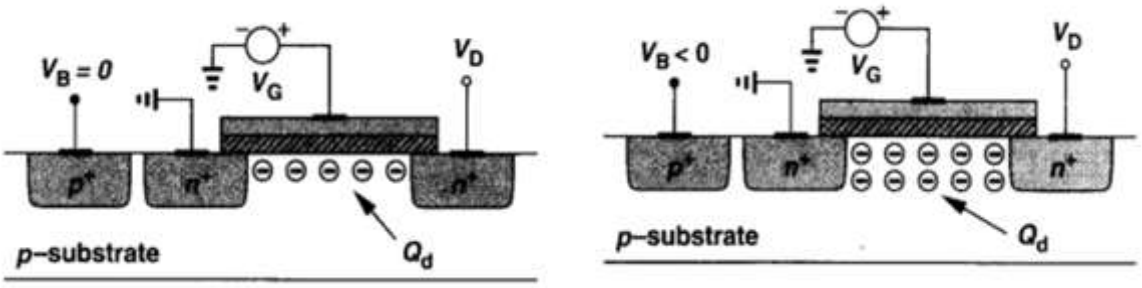


Figure 2.3 Variation of depletion region charge with bulk voltage change

In order to return the same channel depth, the $\mathfrak{r}_{\dagger hm}$ must increase accordingly to threshold voltage increases

2.1.3.2 Channel-length modulation

When the MOSFET enters the saturation region , $\mathfrak{r}_{gm} > \mathfrak{r}_{\dagger hm} - \mathfrak{r}_{n\dagger}$, the channel pinches off before it makes contact with the drain.

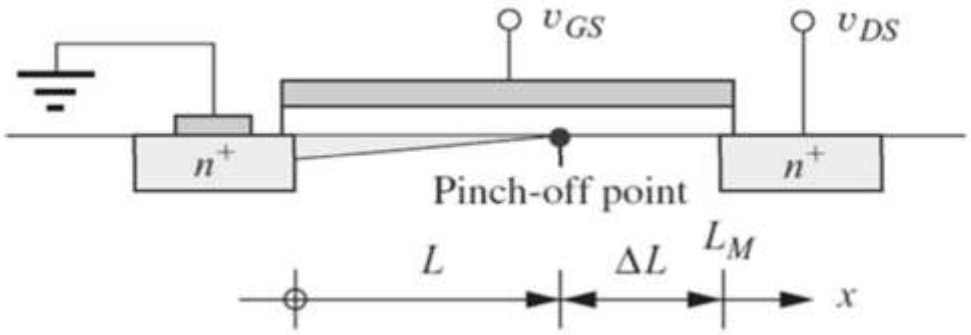


Figure 2.4 Channel-length modulation

The actual length of the resistive channel is given by $\text{ʊ} = \text{ʊ}_\text{ŋ} - \Delta\text{ʊ}$. As $\text{ɾ}_\text{ʂmɻ}$ increases above $\text{ɾ}_\text{ʂmɻsɳ}$, the length of the depleted channel region ʊ also increases, and the effective value of ʊ decreases. The channel length modulation has a significant impact on the drain current that drain current increases as $\text{ɾ}_\text{ʂmɻ}$ increases. The drain current was affected by the channel length modulation can be modeled:

$$\text{ŧ}_\text{ʂ} = \frac{\text{ʊ}_\text{ɯ}^\text{r}}{2}\frac{\text{Ş}}{\text{ʊ}}(\text{ɾ}_\text{ŧhmɻ} - \text{ɾ}_\text{ɳɻ})^2(1 + \lambda\text{ɾ}_\text{ʂmɻ}) \quad (2.5)$$

in which $\chi\acute{\text{C}}$ is called the channel-length modulation parameter

2.1.3.3 Sub-threshold Conduction

In MOSFET model, we assume that current flows from source to drain only when $\text{ɾ}_\text{ŧhmɻ} > \text{ɾ}_\text{ɳɖɻ}$, but in reality the formation of the channel is a gradual effect, therefore, even when $\text{ɾ}_\text{ŧhmɻ} < \text{ɾ}_\text{ɳɖ}$, there is a **weak inversion** layer formed and a small leakage current flows from drain to source. The impact causes a significant increase in the power consumption**.**

2.2 Basic analog circuits

2.2.1 Current mirror

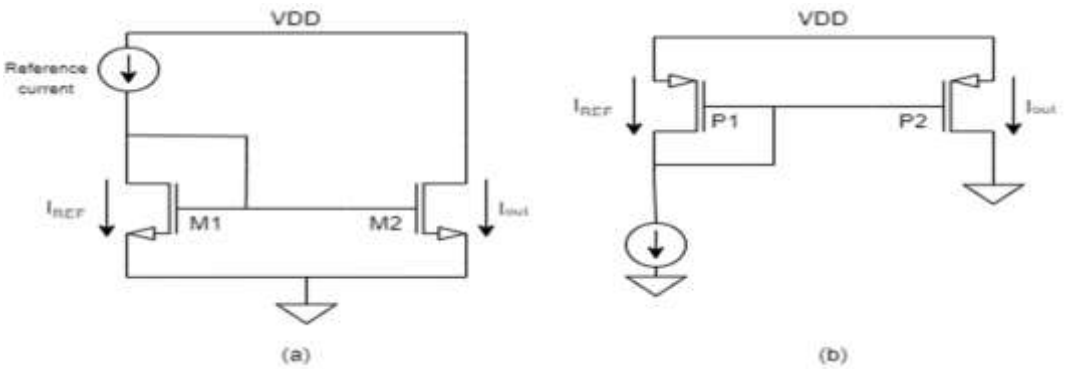


Figure 2.5 Basic current mirror using (a) NMOS and (b) PMOS.

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading.

The current being "copied" can be, and sometimes is, a varying signal current. Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well. Or it can consist of a current-controlled current source (CCCS). The current mirror is used to provide bias currents and active loads to circuits. It can also be used to model a more realistic current source (since ideal current sources don't exist).

An important feature of the current mirror is a relatively high output resistance which helps to keep the output current constant regardless of load conditions.

Another feature of the current mirror is a relatively low input resistance which helps to keep the input current constant regardless of drive conditions. The current being 'copied' can be, and often is, a varying signal current. The current mirror is often used to provide bias currents and active loads in amplifier stages.

In the general case, the transistors need not be identical. Neglecting channel-length modulation, we can write:

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}_1 (V_{GS} - V_{TH})^2 \quad (2.6)$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}_2 (V_{GS} - V_{TH})^2 \quad (2.7)$$

Obtaining:

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF} \quad (2.8)$$

The key property of this topology is that it allows precise copying of the current with no dependence on process and temperature. The translation from I_{REF} to I_{out} merely involves the ratio of device dimensions, a quantity that can be controlled with reasonable accuracy.

2.3 FinFET Technology:

Since Moore's Law, proposed by Gordon Moore, predicted that the number of transistors in integrated circuits would grow faster and become cheaper over time, more than 50 years have passed. During that time, the size of transistors has developed so rapidly that it is now approaching physical limits.

Previously, the transistors in processors were still planar structures created on the surface of silicon wafers. Each transistor (FET – field-effect transistor) has a source terminal, a drain terminal, a channel connecting the source and drain, and a gate located above the channel to control the current flowing through it. In this planar structure, only the gate and a thin dielectric layer between the gate and the channel are placed on top of the silicon.

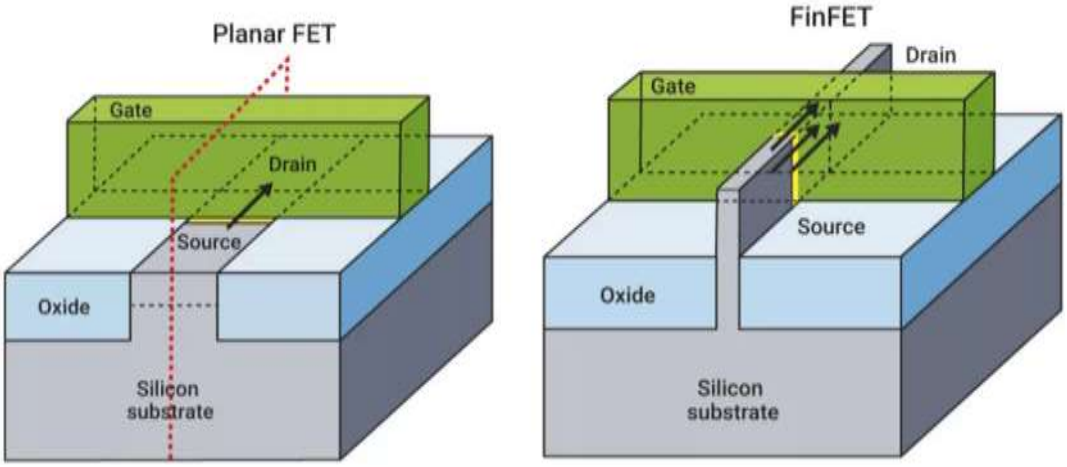


Figure 2.6 Planar FET (left) and FinFET (right)

In the past decade, manufacturers have shifted from planar transistors to FinFET technology to address leakage current issues as transistor sizes shrink. FinFETs feature a vertical channel shaped like a fin, controlled by a gate on three sides—unlike traditional MOSFETs with gate control on only one side. This design improves gate control, reduces leakage, and enables continued device scaling.

FinFETs also offer several advantages:

- Vertical S/D terminals allow smaller footprints and higher transistor density.
- They mitigate short channel effects, which degrade performance in scaled-down MOSFETs.
- Smaller FinFET nodes reduce leakage current more effectively and lower fabrication costs, as shown in Figure 2.6.

2.4 Layout Theories

Layout is a way of arranging parts of a whole in a logical way. In IC design, Layout is to arrange components and draw layer masks representing layers on the IC. In fact, MOSFET operation is influenced by many different physical factors called Layout nonideal factors. Therefore, the layout engineer needs to limit these non-ideal factors to ensure the stable operation of the circuit.

In general, there exist three categories of non-ideal factors within the actual layout: Systematic factors, Random factors, and Gradient factors.

2.4.1 Systematic factor

2.4.1.1 Parasitic capacitance

Parasitic capacitance refers to an inherent and typically undesired form of capacitance that arises due to the proximity of different parts within an electronic component or circuit.

In practical circuits, the presence of parasitic capacitance is unavoidable. The MOSFET itself exhibits parasitic capacitance because of its unique structure as shown in Figure 2.7(a). In Figure 2.7(b) and 2.7(c), the capacitance between the Gate and the Drain (z_5/z_{thg}) originates from the metal barrier created by the insulating oxide layer. The capacitance between the Source and the Substrate (z_1/z_{mt}) along with the Drain (z_2/z_{gt}), is caused by the depletion region formed between them. During the chip fabrication process, the overlap phenomenon contributes to the capacitance between the Gate and the Source/Drain. There is also capacitance between the gate and the channel (z_6), the capacitance between the channel and the substrate (z_3), this is presented (z_{tht}) in Figure 2.7 (b).

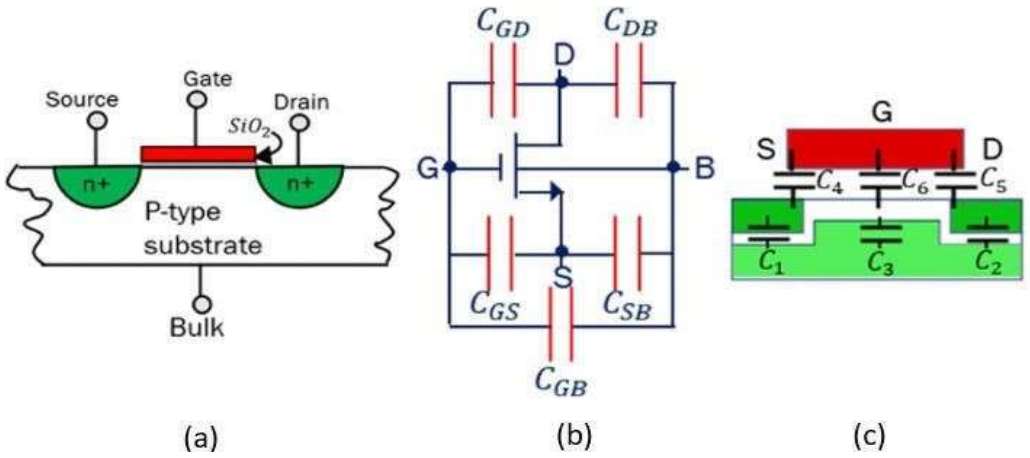


Figure 2.7 (a) MOSFET structure (b) Parasitic capacitances present in Schematic of MOSFET (c) Parasitic capacitances present in cross section of MOSFET

Parasitic capacitances can arise not only within the MOSFET but also directly on the metal lines during the wire layout and routing process. This occurs when two wires run parallel to each other or intersect, separated by insulating material. To overcome this phenomenon, Layout engineer often use shielding techniques to separate the two wire plates.

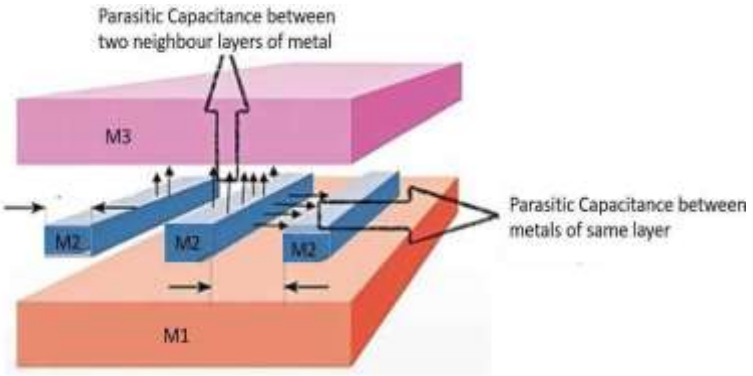


Figure 2.8 Parasitic capacitance from sides of metal and from top and bottom of metal

2.4.1.2 Parasitic resistance

Like parasitic capacitance, parasitic resistance is also inevitable in circuit design. Parasitic resistance exists on contacts and metal layers connecting MOSFETs, and it also exists within the MOSFET itself. Parasitic resistance on interconnects can be mitigated by adjusting the routing strategy, such as increasing or decreasing the width of metals, or by routing in a way that minimizes the wire length.

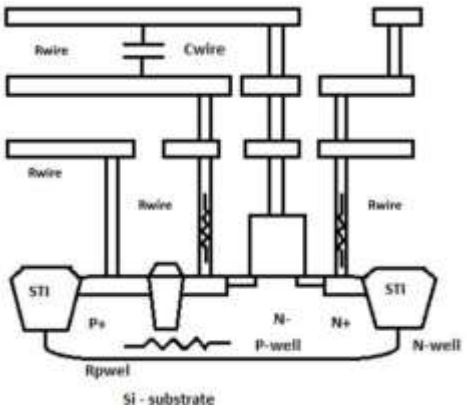


Figure 2.9 Parasitic resistance on wire and MOSFET

2.4.1.3 Shallow trench isolation (STI) stress

During the chip fabrication process, the creation of the oxide layer and Shallow Trench Isolation (STI) requires high temperatures. However, when the chip subsequently cools down to room temperature, the coefficient of thermal expansion for silicon (Si) is significantly higher than that of silicon dioxide (SiO_2). This discrepancy restricts the expansion of the chip due to the presence of the STI layer, leading to a phenomenon known as STI stress.

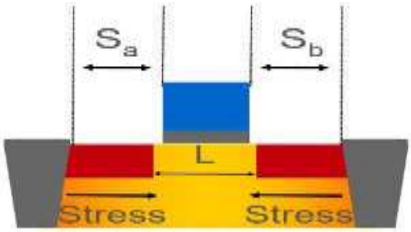


Figure 2.10 STI stress phenomenon

Consequently, these changes in the diffusion region thus change the density of electrons and holes, result in variations in the threshold voltage (V_{th}) and drain current (I_D), which can affect the overall performance of the chip. To overcome this problem, dummy devices can be placed at the edge of the chip, which prevents the main MOSFET from being directly affected by stress.

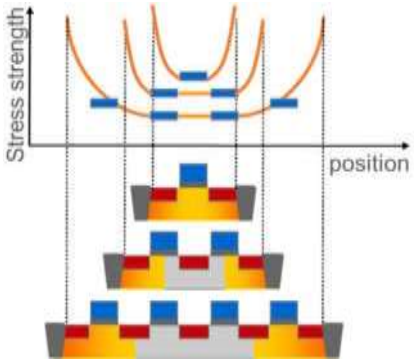


Figure 2.11 STI stress decreases as the distance between the device and the STI increases

2.4.1.4 Well-proximity

During the chip manufacturing process, ion implantation is a common method to create n-well or p-sub structures. In this method, ion beams are directed towards the target region at an angle typically ranging from 7 to 9 degrees. However, it is possible that some of these ion beams may accidentally hit the photoresist layer, which is used for photolithography, and reflect onto the substrate. As a result, the impurity concentration in the region of the substrate can differ from that of the central region. To overcome this problem, dummy devices can be placed at the edge of the chip.

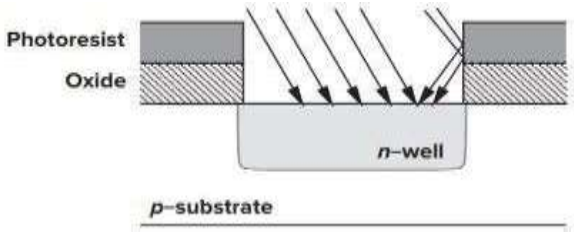


Figure 2.12 Well Proximity Effect

2.4.1.5 Pattern non-uniformity

During the photolithography process, when UV light passes through the mask layers to harden or soften the photoresist layer, the intensity of light exposure in the center is higher than at the edges due to light diffraction. As a result, the photoresist outside the edges of the chip has a different level of hardness or softness compared to the center. This difference causes variations in the region within the desired region of the chip. To overcome this problem, Layout engineer often place dummy devices at the edge of the chip to increase the light intensity of the main part of the chip.

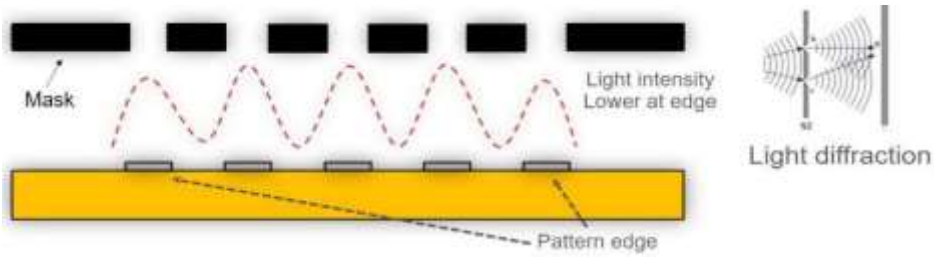


Figure 2.13 Pattern non-uniformity phenomenon

2.4.1.6 S/D Asymmetry

The two terminals S and D of a MOSFET are not perfectly symmetrically positioned with respect to the Gate as predicted by theory, resulting in deviations. These deviations are caused by the angled ion implantation process. If the implantation is angled from S to D, the S terminal will overlap below the G terminal, while the D terminal will deviate away from the G terminal, and vice versa.

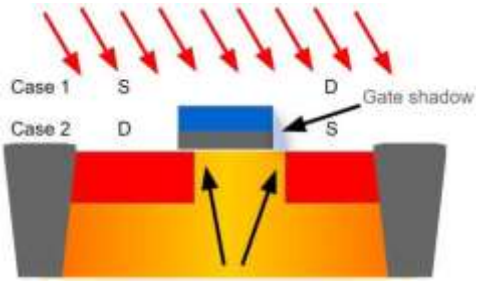


Figure 2. 14 S/D Asymmetry phenomenon

2.4.2 Gradient Factors:

In non-ideal condition, it contain many changings of physical parameter effecting to potential property of devices called gradient factor. Example: temperature, process variation, etc. They are inevitable so in layout step, we must consider this phenomenon to ensure the performance of the matching pair.

Gradient factor divides to 2 types:

2.4.2.1 Linear type.

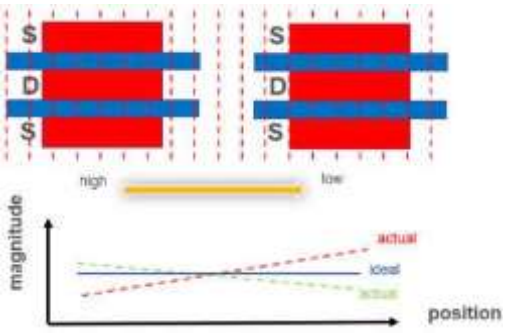


Figure 2.15 Gradient change

Following Fig 2.15, linear type of gradient change is the changing follow the certain orientation with the linear magnitude. Comparing to idea condition, the magnitude of the changing physical parameters is homogeneous for both devices while non – idea case isn't. It may cause the different working principle of each device in matching pair.

2.4.2.2 Non-linear type.

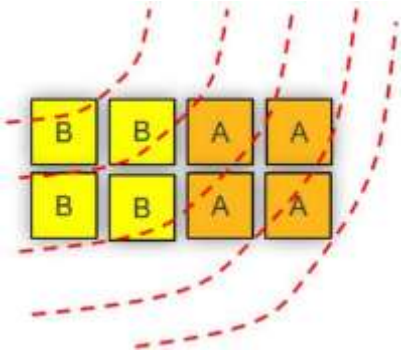


Figure 2.16 Non-linear change

Non-linear change has the same meaning with the linear change, it also effecting on the function of the devices but the way it effects not govern by any linear rule.

2.5 Layout Technique:

As mentioned in Part 2.4 (Layout Theories), all the Systematic factors are inevitable because they occur mainly during the chip manufacturing stage. But in layout

design, we have a few techniques that, although they cannot completely overcome those weaknesses, can reduce their impact on this design.

2.5.1 Reducing effects of parasitic capacitor

Following to chapter 2.4.1.1, we are mentioned about parasitic capacitor appear in routing process. This presence of unwanted component causes the coupling noise for the amplitude of signal alleviate the trust of the circuit. In this case, shield is adding to the middle of couple signal has different phase.

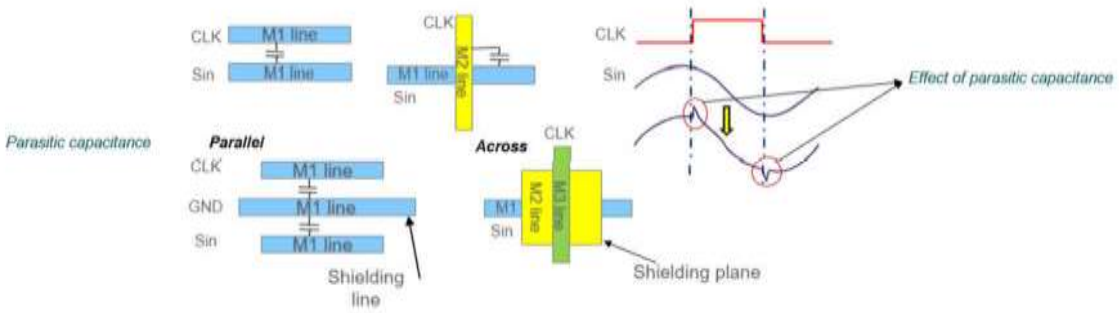


Figure 2.17 Effect of parasitic capacitor on signal

Consider shielding, it is the normal metal wire place at the middle of couple different phase signal which has the value of signal is stable (frequently is power signal). Adding shield method lend us the hand to protect the couple of critical signals by the transferring noise to shielding which we do not use.

In the case routing signal, parasitic capacitor contributes to tumbling the performance of the circuit so the best solution to deal with them is shortest routing for signal metal.

Note: Adding shielding for matching pair signal must be consider the spacing from shield to signal metal to ensuring the value of parasitic capacitor is equal.

In terms of matching pair signal, parasitic capacitor must be considered carefully on both matching signals to make sure both has the same working condition.

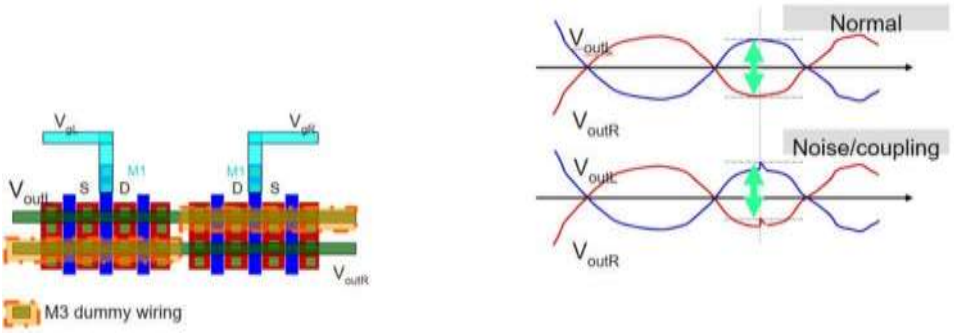


Figure 2.18 Dummy Wiring

In this case, dummy wiring is adding to ensuring the matching pair signal has receives the same noise to protect their function.

2.5.2 Reducing layout effects:

In the chapter 2.4.1 and 2.4.2, there are many layout effects has repercussion on performance of our circuit. In this case, dummy components are adding. In terms of this project, dummy components we use are dummy gates, active dummy devices.

Active dummy devices are the devices with source and drain connecting with signal or power has the same properties, gate of active dummy must connect with power/ground to make sure this device turns off.

Adding dummy devices can reduce effect of STI stress, WPE, Pattern non uniform. In the case STI stress, we can add dummy devices with sharing diffusion.

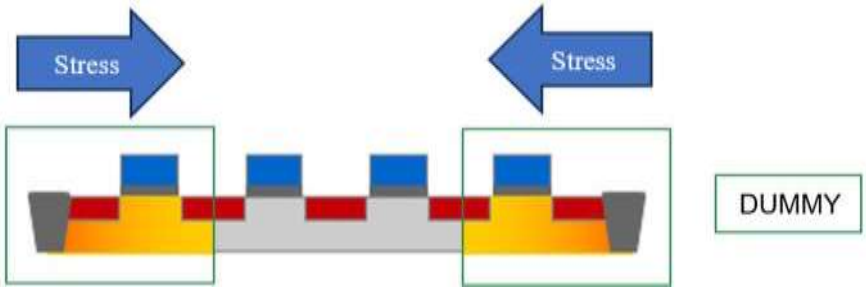


Figure 2.19 Reducing STI stress

The forces of STI stress mainly effects on the dummy devices and it reduce the amplitude when meeting the real devices. In addition, dummy devices can solve the well proximity problem.

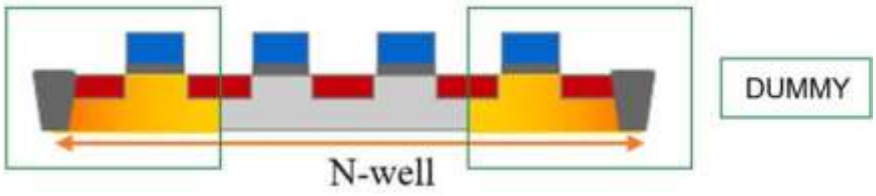


Figure 2.20 Reducing WPE

Following the Figure 2.20, It illustrates that the region of Nwell is expanded at both edge of real devices by adding dummy devices hence, we can ensure that our real devices has spacing to well edges. In terms of pattern non uniformity, dummy devices are also deal with this problem, dummy gates can do it too.

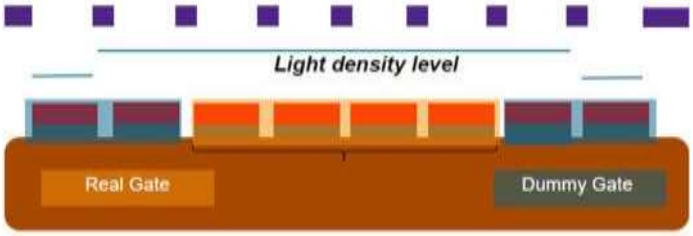


Figure 2.21 Avoid pattern non uniformity

Through the fabrication process, adding dummy help us ensuring that the light density consumption of real devices is homogeneous.

2.5.3 Guard Ring/Tap

An n-well, the p-substrate, and another n region form a parasitic NPN transistor in a CMOS-based integrated circuit using the p-substrate, which could be turned on when one of the PN junctions in the transistor is forward-biased, causing latch-up of a device on the integrated circuit or even permanently damaging the integrated circuit. Latch-up occurs when a circuit draws unmanageable current and specific voltages are driven, or "latched-up", to an unwanted and uncontrollable level that violates the circuit's working requirements. Crosstalk between devices in an integrated circuit is the most common cause of latch-up circumstances. Bipolar integrated circuits, as well as field-effect transistors like MOSFETs, have undesirable crosstalk between devices.

Guard-ring/tap is used to prevent current leakage from one component to another: n+ guard-ring/tap for PMOS and p+ guard-ring/tap for NMOS help intercept minority

carrier diffusion and either block or extract them (electrons go into n+ regions, holes go into p+ regions) as shown in figure 2.22

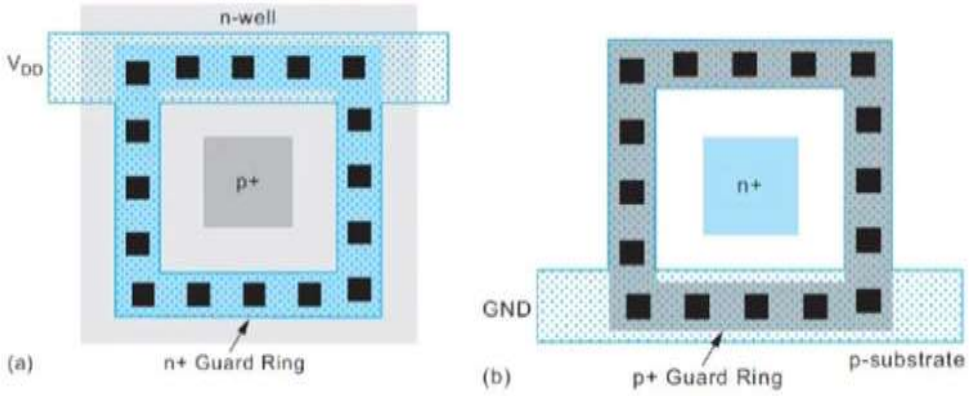


Figure 2.22 (a) n+ guardring (b) p+ guardring

2.5.4 Balance Gradient Factor

2.5.4.1 Interdigitation Technique

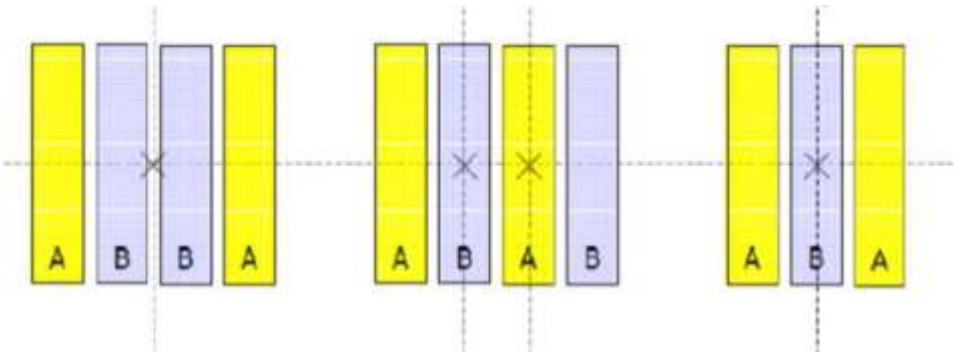


Figure 2.23 Interdigitation technique

The interleaving technique is employed to ensure that components remain matched under the influence of gradient factors such as temperature, pressure, and others. This arrangement technique can eliminate linear gradient effects when these external influences vary across different components

2.5.4.2 Symmetric Technique

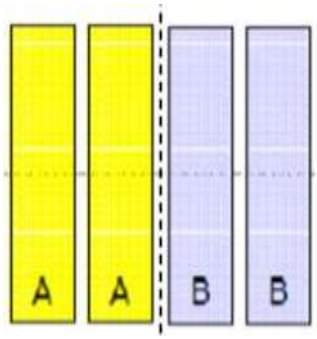


Figure 2.24 Symmetric Technique

The symmetric layout technique is employed in analog design to ensure that devices remain well-matched when subjected to bilateral effects such as STI stress, well proximity effects, and similar layout-dependent phenomena, ... However, this technique cannot eliminate linear gradient effects when the external influences on the components differ.

2.5.4.3 Common Centroid Technique

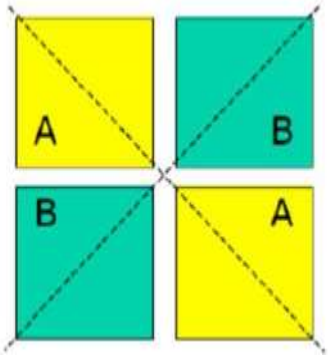


Figure 2.25 Symmetric Technique

The common-centroid layout technique is also employed to enhance matching between devices. It can effectively eliminate both linear and non-linear gradient effects, ensuring that external influences are distributed more uniformly across the components. However, this technique presents challenges in terms of routing complexity and connecting to polysilicon gates.

2.5.5 Physical Verification

Designers must follow some physical verification (PV) to check the design quality such as layout versus schematic check (LVS) and Design Rule Checking (DRC).

2.5.5.1 LVS

LVS extracts the electrical connectivity from the physical layout, and then compares the physical layout connectivity and device properties to that of the schematic. The comparison check is considered clean if the physical layout implementation matches the design intent of the schematic circuit design.

Two main processes make up the LVS flow. The first process in the flow is extraction, in which the layers within the layout database are analysed and all the devices and nets are extracted. The second process in the flow is compare, in which the actual comparison of devices and nets occurs.

The LVS runset contains a series of function calls that control both extraction and netlist comparison.

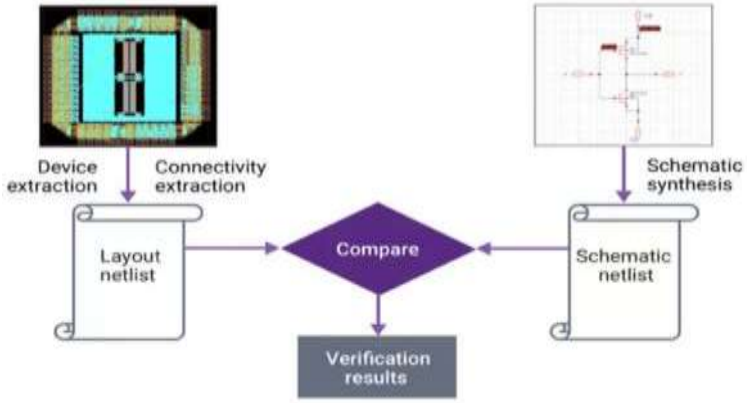


Figure 2.26 LVS diagram

2.5.5.2 DRC

DRC checks whether a physical design complies with the process technology's design standards. It is an important aspect of the physical design process since it assures that the design fits production standards and will not fail.

There will be restrictions specific to each process technology. The DRC engine compares the physical arrangement geometry to the ICV rule deck's design rules.

- Minimum width
- Minimum spacing
- Minimum area
- Wide metal jog
- Misaligned via wire

- Special notch spacing
- End-of-line spacing

2.6 Chapter Conclusion:

In conclusion, this chapter has presented a comprehensive literature review on CMOS technology. By exploring the basic concepts in the semiconductor industry, the fundamental theories of CMOS, the layout theories and layout techniques associated with this technology, we have gained valuable insights into the principles underlying CMOS design and fabrication. Overall, this literature review establishes a strong foundation for further research and development in CMOS technology.

CHAPTER 3: PROPOSED PHYSICAL DESIGN FOR HIGH-SPEED DUTY CYCLE DETECTOR

In this chapter, we will go into detailed exploration of the schematic diagram and functions, as well as the physical design, of the two blocks in the Duty Cycle Detector circuit as mentioned in Chapter 1, which include **Bias Current** and **Folded Cascode**.

3.1 Circuit diagram and working principle

3.1.1 Current Source

To ensure stable operation across all PVT corners, it is necessary to design a bias current source that is less sensitive to variations in VDD and resistor values.

Therefore, the threshold voltage-referenced current source is selected. As discussed in Chapter 1, this circuit depends primarily on the r_{thm} of the reference transistor N15.

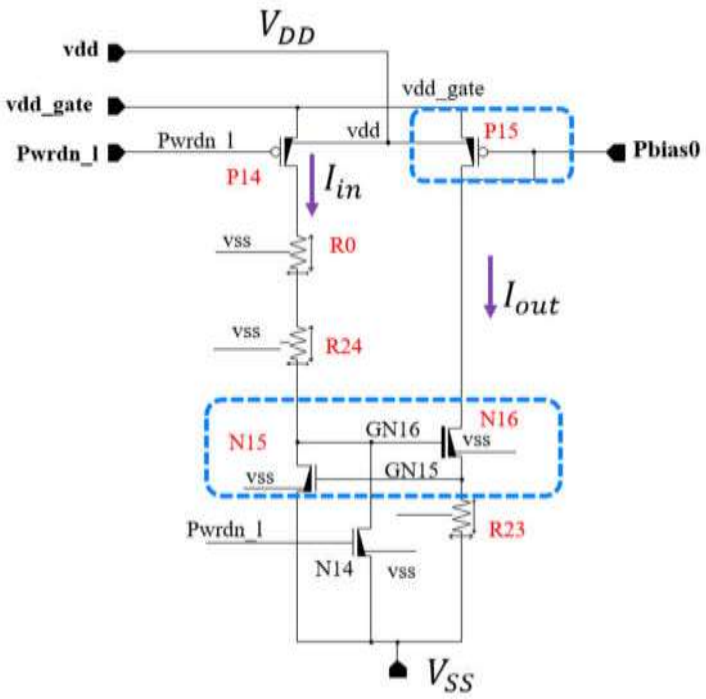


Figure 3.1 Threshold referenced current source

Function of each device in the circuit:

- PMOS P14 and NMOS N14 act as switching elements.
- NMOS N15 is responsible for generating the input current I_{td}.
- Resistors R0 and R24 serve as bias resistors for NMOS N16, and together with N15, form the path that generates I_{td}.

- Resistor R23 works in conjunction with NMOS transistors N15 and N16 to generate I_{bias}. The V_{thn} of N15 is the primary reference for creating the output current, while R23 also functions as the bias resistor that ensures N15 operates in the desired region.
- PMOS P15 is a current mirror that replicates I_{bias} and supplies the bias current to the preamplifier stage.

Working Principle

When the Pwrdn_l pin is set to 0, PMOS P14 conducts while NMOS N14 is turned off. With VDD applied, an input current I_{id} is generated, creating a voltage drop at the gate of NMOS N16. As a result, N16 conducts and produces the output current I_{bias}. This I_{bias}, in combination with resistor R23, provides biasing for NMOS N15.

Conversely, when P14 is turned off, VDD is disconnected from the circuit, and N14 pulls the gate of N16 down to VSS, turning off N16, resulting in $I_{id} = I_{bias} = 0$.

$$I_{bias} = \frac{V_{thn15}}{R_{23}} = \frac{V_{n15} + V_{GS15}}{R_{23}} = \frac{V_{n15} + \sqrt{\frac{2I_{id}}{\mu_n C_{ox}(W/L)_{n15}}}}{R_{23}} \quad (3.1)$$

3.1.2 Current Mirrors:

To provide biasing for each transistor in the circuit, a current mirror structure is used to copy the bias current source in Section 3.1.1 and distribute it to the transistors in the folded cascode preamplifier stage.

In the preamplifier stage, a folded cascode differential structure is employed. Therefore, it is necessary to replicate four bias voltage levels from the bias current source described in Section 3.1.1.

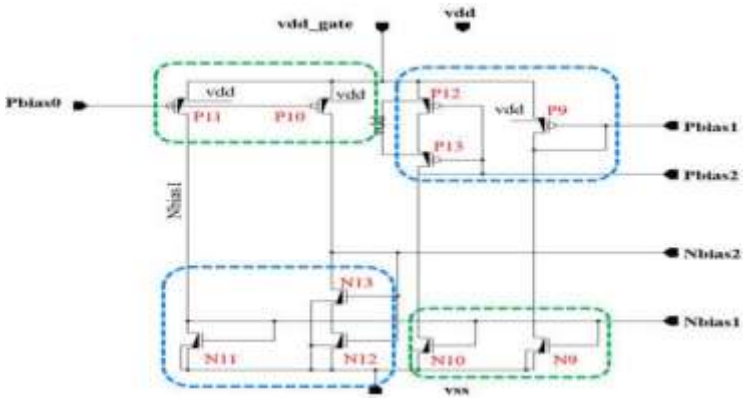


Figure 3.2 Current Mirrors Schematic

Function of each device in the circuit:

- Transistors P9, P12, P13, N11, N12, and N13 are referred to as reference transistors,
- while transistors P10, P11, N9, and N10 are considered mirroring (copy) transistors.

Working Principle

From the previous current source stage, the current ŧª\ªbªaenters the Pbias0 node.

P11 and P10 sequentially copy the Iout current to generate mirrored current branches through P11–N11 and P10–N12–N13.

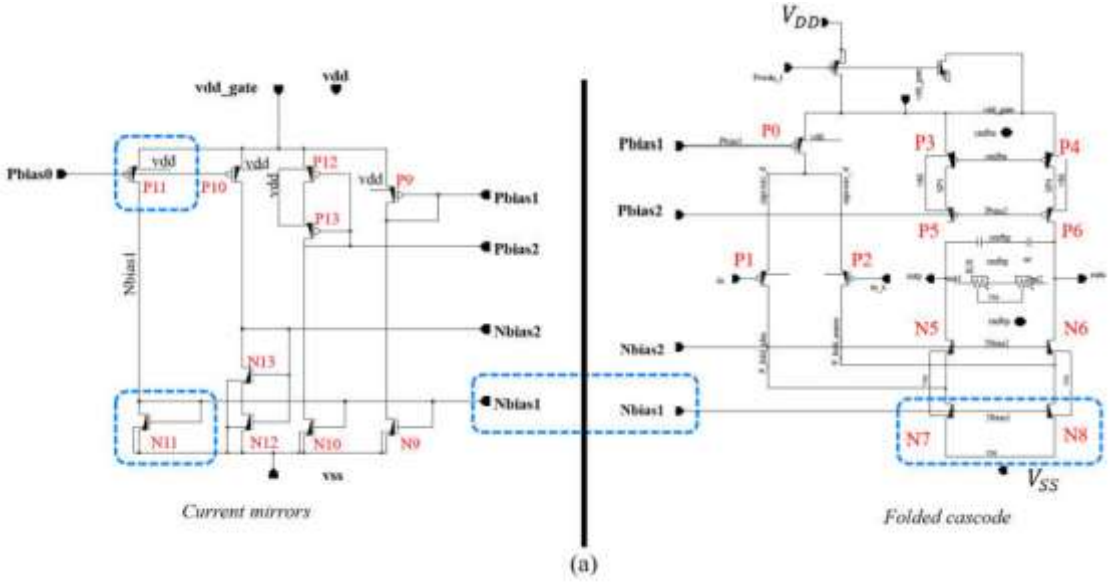
Transistor N11 and the pair N12–N13 are configured as diode-connected transistors to receive the current from P11 and P10, creating two bias voltages: Nbias1 and Nbias2.

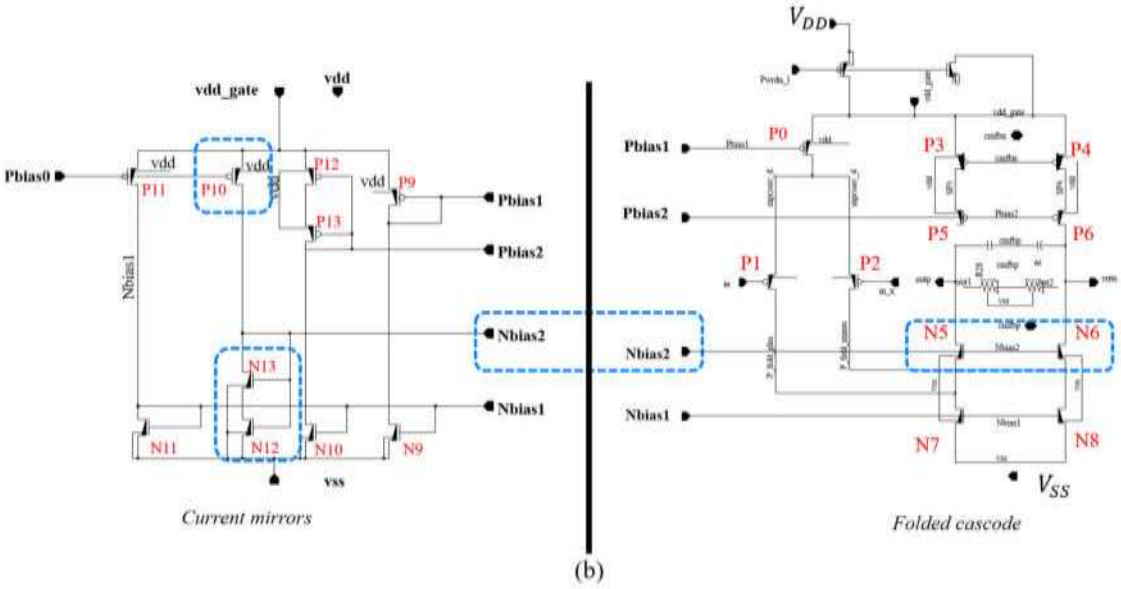
Similarly, N9 mirrors the current of the P11–N11 branch via reference transistor N11,

and N10 also mirrors this current through N11 as the reference.

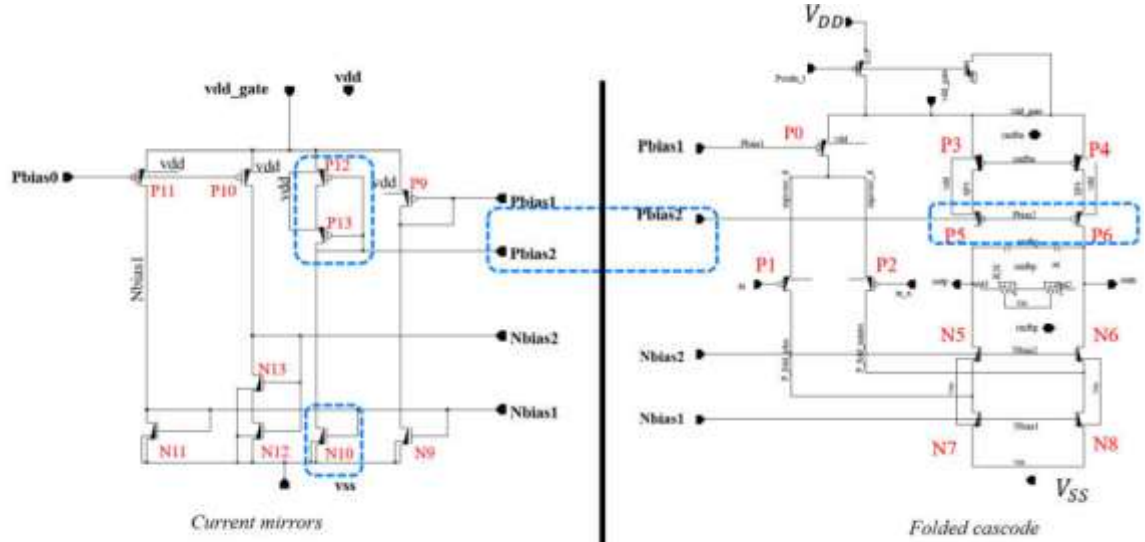
Transistor P9 and the pair P12–P13, also diode-connected, produce two additional bias voltages, Pbias1 and Pbias2.

At this point, four different bias voltages: Pbias1, Pbias2, Nbias1, Nbias2 are generated to bias the transistors in the folded cascode preamplifier stage.




vdd_gate
vdd
Pbias0
P11
P10
P12
P9
P13
Pbias1
Pbias2
Nbias1
Nbias2
N13
N11
N12
N10
N9
vss
Current mirrors
V_{DD}
P0
P3
P4
P1
P2
P5
P6
N5
N6
N7
N8
V_{SS}
Folded cascode

(b)


vdd_gate
vdd
Pbias0
P11
P10
P12
P9
P13
Pbias1
Pbias2
Nbias1
Nbias2
N13
N11
N12
N10
N9
vss
Current mirrors
V_{DD}
P0
P3
P4
P1
P2
P5
P6
N5
N6
N7
N8
V_{SS}
Folded cascode

(c)

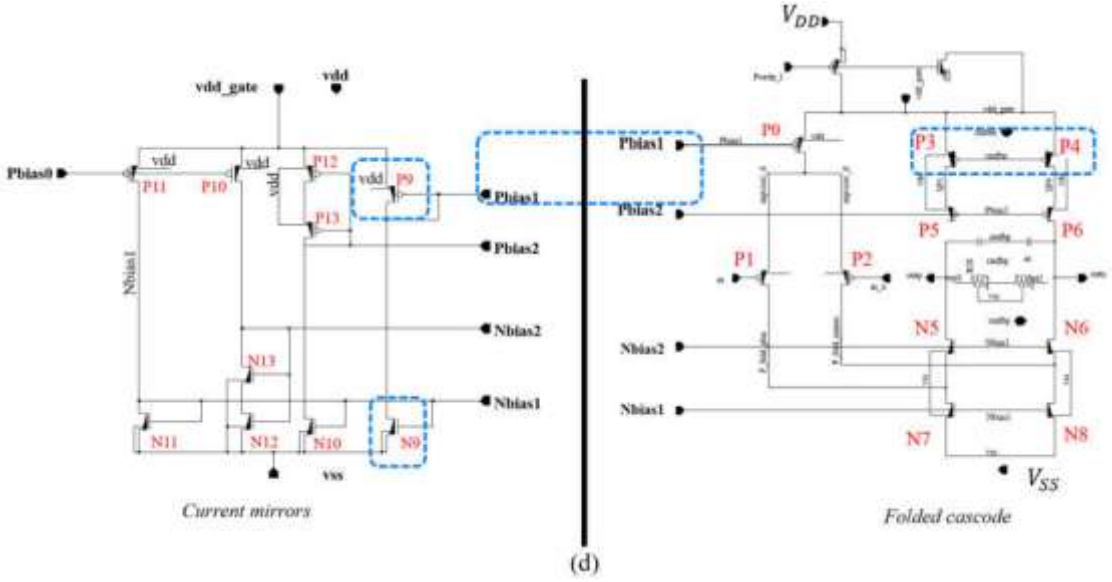


Figure 3.3 Bias Current Mirrors for the Folded Cascode Block: (a) Nbias1 (b) Nbias2 (c) Pbias2 (d) Pbias1

3.1.3 Folded Cascode

To amplify the difference between two signals, a differential amplifier is required. For basic differential amplifier circuits with resistive load (R_D), the voltage gain is given by $A_v = -g_m R_D$, which requires a trade-off between gm and R_D. As a result, such circuits often cannot achieve the desired gain.

On the other hand, when using diode-connected loads, current loads, or conventional cascode loads, the output swing is limited by V_{th} and V_{dsat}, leading to a common-mode voltage at the output that may not meet requirements.

Therefore, a folded cascode differential amplifier structure is used to overcome the limitations and effectively amplify the signal difference between two inputs.

This is the reason why the folded cascode differential amplifier architecture is adopted.

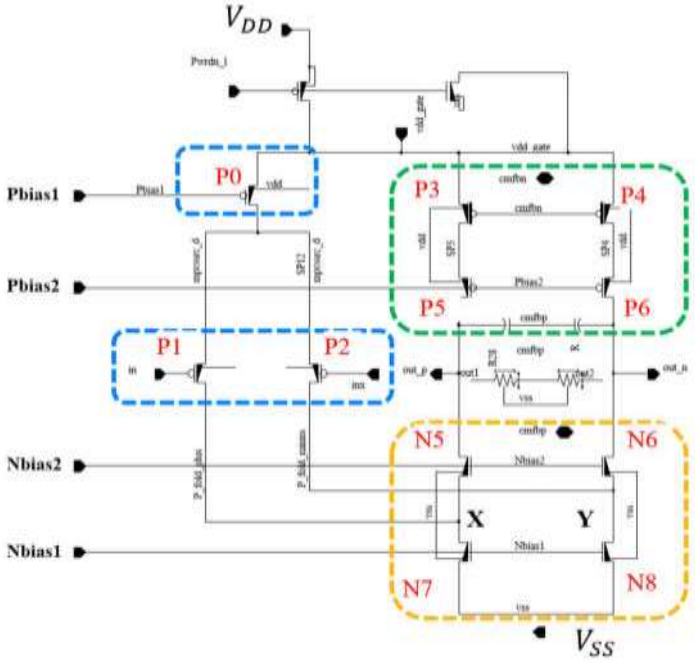


Figure 3.4 Folded Cascode Schematic

Function of each device in the circuit:

- The input PMOS pair P1 and P2 forms the differential input pair, which is the core component of the circuit responsible for amplifying the differential signal between the two inputs in and inx.
- PMOS P0 functions as a current source that supplies current and provides biasing for the differential input pair.
- PMOS pairs P3–P4 and P5–P6 serve as cascode loads, increasing the output impedance of the circuit. In particular, the gates of P3 and P4 also act as the negative feedback input of the circuit.
- NMOS transistors N5 and N6 function as current sources, and at the same time, they constitute the folded cascode stage of the circuit.
- NMOS transistors N7 and N8 operate as a bias current source for the entire cascode stage and carry the total current of the circuit.
- Resistors R1 and R2, together with the Miller capacitors C1 and C2, form a Common Mode Feedback (CMFB) loop. They sense the common-mode voltage at the output and feed it back to bias the gates of P3 and P4.

Working Principle

- When r_{td} increases, the $|r_{thm}|$ of P1 decreases, causing $|t_{g1}|$ to drop. As a result, the voltage at node X (r_{f}) decreases, which increases the r_{thm} of

N5, making N5 conduct more strongly. Consequently, the current through the cascode branch increases, and the output voltage V_{out} decreases. Thus, the output signal is inverted relative to the input signal.

- Similarly, when V_{in} increases and $|I_{D1}|$ decreases while the bias current from PMOS P0 remains constant ($I_{bias} = |I_{D1}| + |I_{D2}|$) ,the current $|I_{D2}|$ must increase. This causes the other cascode branch to operate in the opposite direction, resulting in V_{out} increasing.
- Conversely, if V_{in} decreases, then V_{outp} increases; $|I_{D2}|$ decreases, and V_{outn} decreases.

3.2 Layout Design

The layout of DCD includes main blocks: RC Filter, Reference Voltage, Folded Cascode, Strong Arm latch, Bias Current, SR_trigger. In the scope of this thesis, only the Bias Current and Folded Cascode blocks are implemented and laid out.

The size of DCD (Bias Current and Folded Cascode) is 20.84 µm × 22.547 µm and its area is 469.88 µm^2. Between Bias Current and Folded Cascode, the folded cascode is the most important because it affects and determines a lot on result of DCD circuit, so in the Folded Cascode block we need to apply various technique such as common centroid, symmetric, dummy guard ring and shielding. It is obvious that in the layout, each transistor has been covered by an OD layer, this is where the guard ring technique is applied to protect the transistor from latch-up effect. According to the guidance from design team at Synopsys, they suggested us that using common centroid structure is better than interdigitated or symmetrical to balance effect of gradient factor such as temperature, process variation on the matching pairs cause mismatch. Therefore, input diff – pairs in comparator block use common-centroid for the sake of balance linear and non -linear factors for matching pairs. Besides, important signals such as in, inx, outn and ounp need to apply shielding method to protect those signals from noise.

To clearly understand the techniques that we have applied in layout design. We will analyze the floorplan and routing of each block in the section below.

3.2.1 TopCell

Based on the schematic, we have Bias Current (Current Source and Current Mirror), Folded Cascode, Decap which uses to help stable the signal. We will apply the technique in part 2.5 to analyze including floorplan and routing important signals in the following table 3.1

3.2.1.1 Floorplan

Table 3.1 Floorplan requirements

Num	Requirement	Yes/No
1	Order of blocks must be followed as below: Folded Cascode, Current Mirror, Bias Current, Decap	Yes
2	Devices are correspondingly placed with the schematic	Yes
3	Devices are as close as possible to optimize area	Yes
4	Be aware of ½ rule for interface	Yes

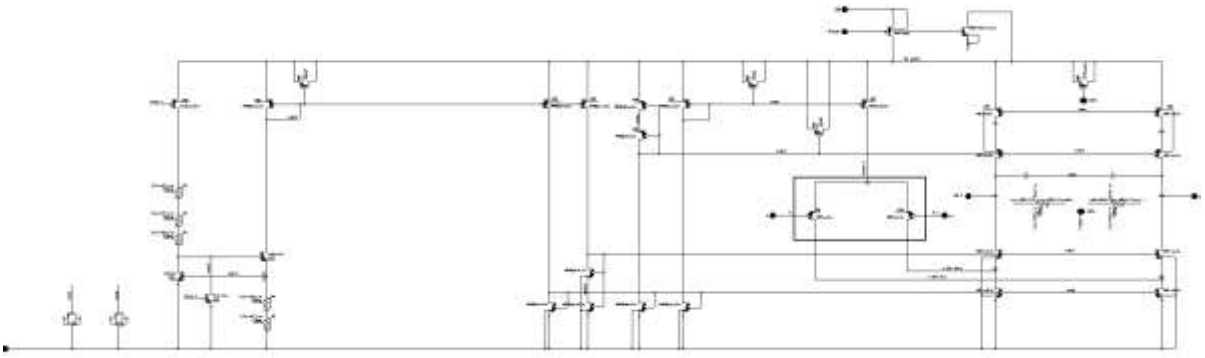


Figure 3.5 General Schematic

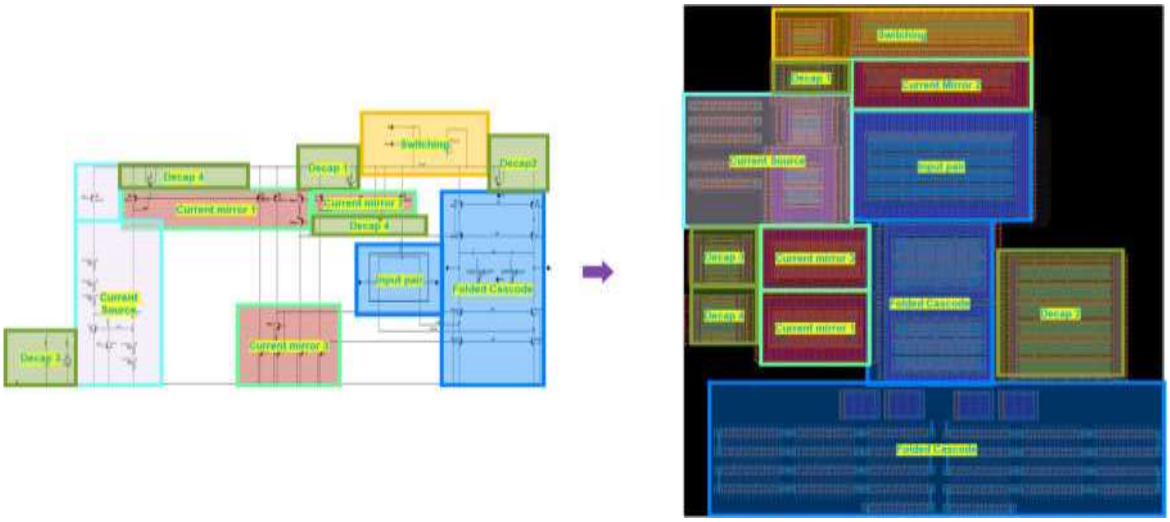


Figure 3.6 Layout of DCD

As shown in Figure 3.6, the organization for each block is also called as the floorplan and this will make sure that device placement is estimated to make it easier and more convenient before moving to the interconnection stage.

In the topcell floorplanning process, the Folded Cascode block was placed first as the reference anchor, since it is the core of the design. Subsequently, the Current Mirror blocks were placed adjacent to the MOS transistors within the Folded Cascode that they are intended to bias. This approach helps minimize IR drop and ensures more stable biasing performance.

Similarly, the Current Source block was positioned close to the Current Mirrors in order to optimize the parasitic resistance in the current path, thereby improving overall current accuracy and reducing voltage loss.

The Decap (decoupling capacitor) blocks were strategically placed near the critical signal lines of the Current Mirror blocks to help stabilize voltage fluctuations and enhance signal integrity. Besides, this arrangement will optimize the smallest possible area

3.2.1.2 Power routing requirements

Table 3.2 Power routing requirements

Num	Requirements	Yes/No
1	Power/Ground is matched with devices floorplan	Yes
2	Add power/ground as much as possible	Yes
3	Power/Ground pins: M7	Yes
4	Ground is balanced with power	Yes
5	Max density of M7 is (78%) – 5% = 73%	Yes

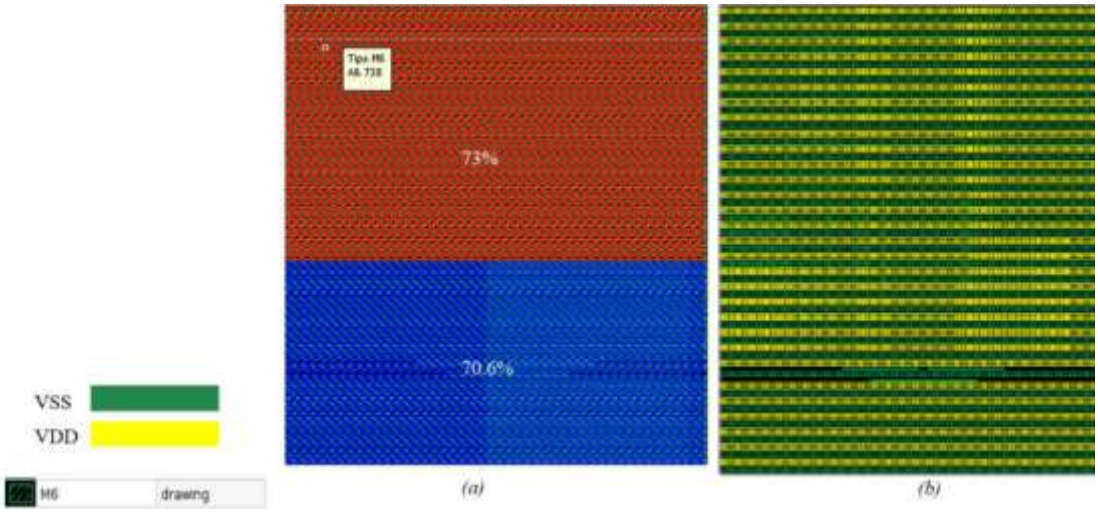


Figure 3.7 (a) M6 Density in Boundary (b) M6 Power Mesh

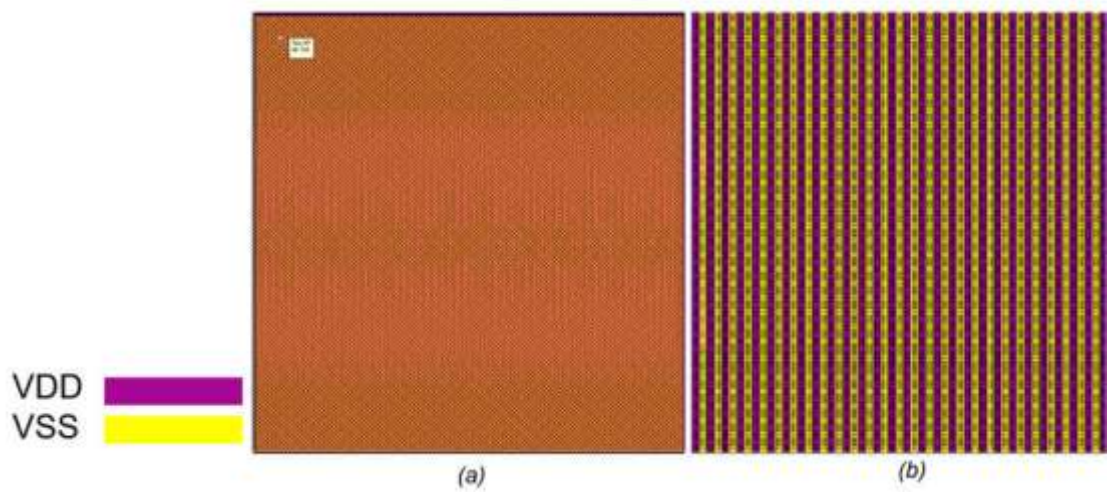


Figure 3.8 (a) M7 Density in Boundary (b) M7 Power Mesh

Table 3.3 Power routing in metal 7

Num	Power	Metal	Width	Length	Spacing	Direction	Quantity	Density
1	VDD	M7	$0.27\mu m$	22.329	0.1	Vertical	28	73%
2	VSS	M7	$0.27\mu m$	22.329	0.1	Vertical	28	

3.2.2 Folded Cascode Block

3.2.2.1 Floorplan requirements

In the duty cycle detector, the folded cascode block plays a crucial role in achieving acceptable performance. Specifically, the diff-pairs are highly sensitive to various factors that can alter the device's potential properties, leading to mismatches. Therefore, it is essential to apply the matching pairs techniques to the diff-pairs, ensuring compliance with the requirements outlined in Table 3.4 & 3.5.

Table 3.4 Floorplan requirements

Num	Requirements	Yes/No
1	Devices in Folded Cascode must be symmetric in Y axis as much as possible	Yes
2	Matching pair must use common centroid	Yes
3	Matching pair must have dummy at both sides (Input pair must have dummy at four sides)	Yes
4	Each matching pair must be placed in separated guard-ring	Yes
5	Drain and source of matching pairs are kept equivalent orientation and the number of D/S and S/D orientation met	Yes

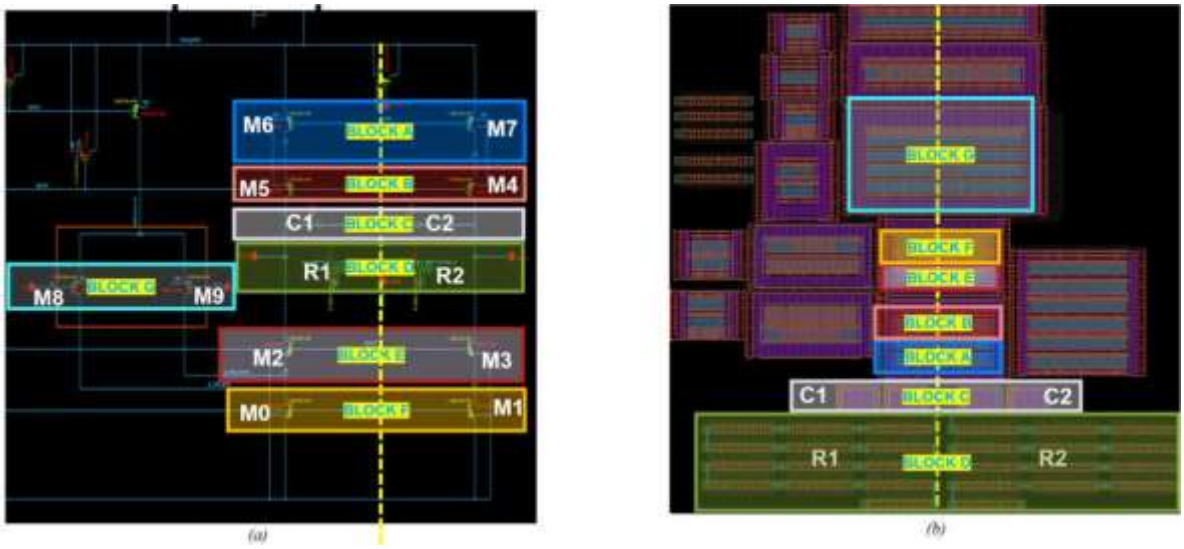


Figure 3.9 (a) Folded Cascode Schematic (b) Folded Cascode Placement

Firstly, we have four main parts:

- Input differential pair: M8, M9
- Cascode loads: M6, M7, M5, M4
- Folded Cascode devices: M2, M3
- Bias Current Sources: M0, M1

All of these parts is crucial part. Therefore, we currently position these devices within an individual guard-ring. Additionally, devices in Folded Cascode must be symmetric in Y axis as much as possible. This is clearly illustrated in Figure 3.10 & 3.11 & 3.12 below

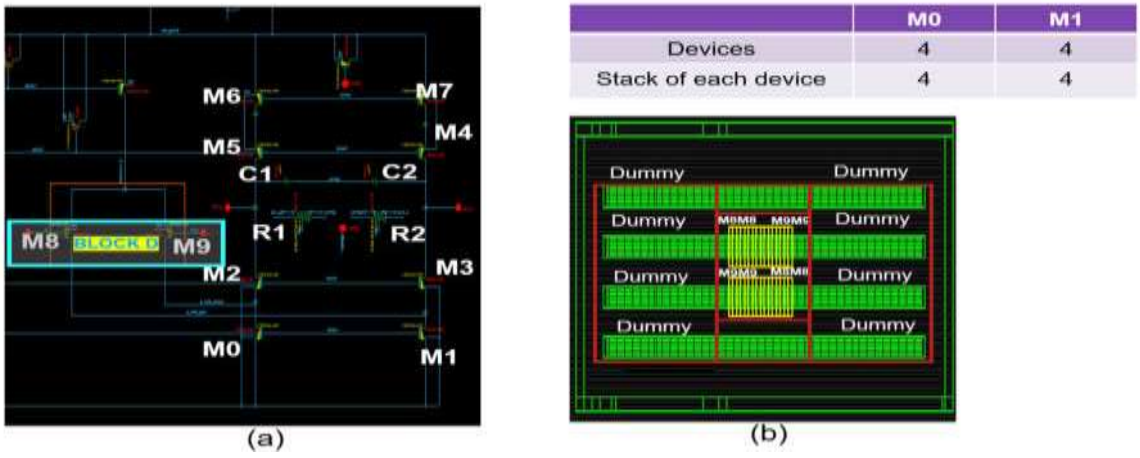


Figure 3.10 (a) Folded Cascode schematic (b) Guardring for input diff-pair

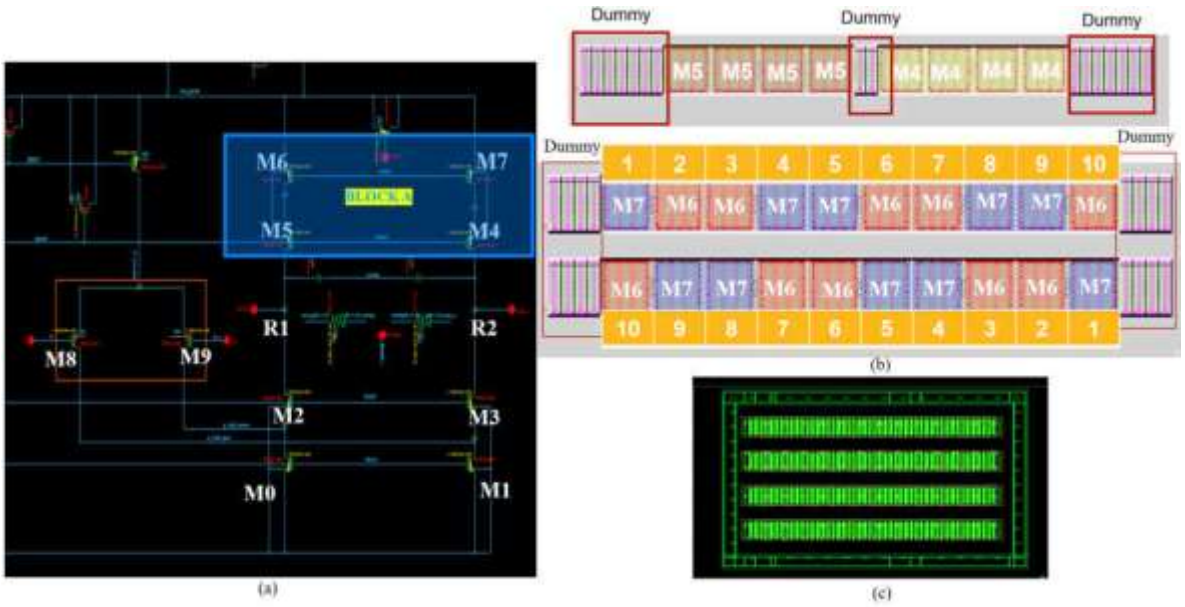


Figure 3.11 (a) Folded Cascode schematic (b) PMOS pair arrangement (c) Guardring for PMOS pair

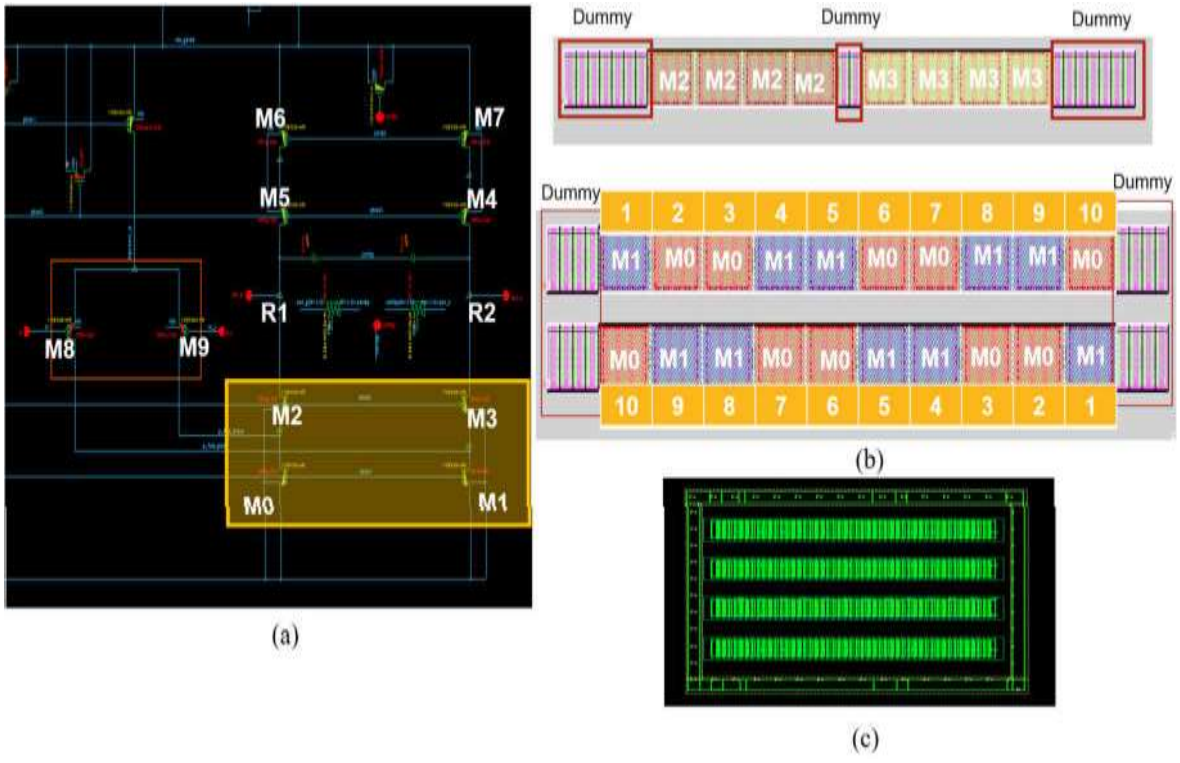


Figure 3.12 (a) Folded Cascode schematic (b) NMOS pair arrangement (c) Guardring for NMOS pair

As shown in Fig. 3.10 & 3.11 & 3.12, we provide a detailed presentation on the common-centroid placement of six transistors, M8 and M9 (input differential pair), and

M6 & M7 pair, M0 & M1 pair enabling them to balance with respect to undesired effects as well as noise impacting the two devices. Meanwhile, M2 & M3 pair and M4 & M5 pair are placed using symmetric technique instead of common centroid because these transistors are relatively small in size, so the impact of layout-induced mismatch is less significant, and Symmetrical placement is sufficient to ensure matching without complicating routing. In addition, guard ring is also covered in this block to suppress the substrate coupling.

Additionally, for semiconductor resistors, special attention must be paid during physical design, as they tend to generate significant heat and electrical noise during operation. These effects can negatively impact both the performance and the reliability of the circuit over time.

Therefore, the resistors are deliberately placed at a distance from sensitive active devices to mitigate thermal and noise interference.

3.2.2.2 Signal routing requirement

In addition to the floorplan requirements, we are also concerned about the critical signals within the folded cascode block, including in, inx, outn, outp. All critical signals must be routed symmetrically with an equal number of contacts. Additionally, shielding is necessary for important signals. Furthermore, there must be a connection to both ends of poly gates to minimize the propagation delay time to active devices.

Table 3.5 Routing requirements

Num	Requirements	Yes/No
1	All the signals of matching pairs must be routed symmetrical	Yes
2	Matching pairs must use symmetrical number of contact	Yes
3	Matching pair must have connection to both ends of Poly gates	Yes
4	Signals outn, outp and in, inx must be shielded with power	Yes
5	Width of critical signals must be passed EM	Yes

The table above summarizes the requirements that we apply in the routing of the folded cascode block. We provide detailed information on each critical signal that requires matching below. Firstly, for the input signals in (blue) and inx (red), they are connected in a way that ensures equal capacitance and resistance values. We have also exported the capacitance values of these two signals in Fig 3.13. They are shielded using VDD lines. However, only the M3 and M4 metal lines are actually shielded, due to limited layout space around the M2 metal line. Moreover, the M2 routing for the in and

inx signals is relatively short, which reduces the risk of interference, making additional shielding unnecessary.

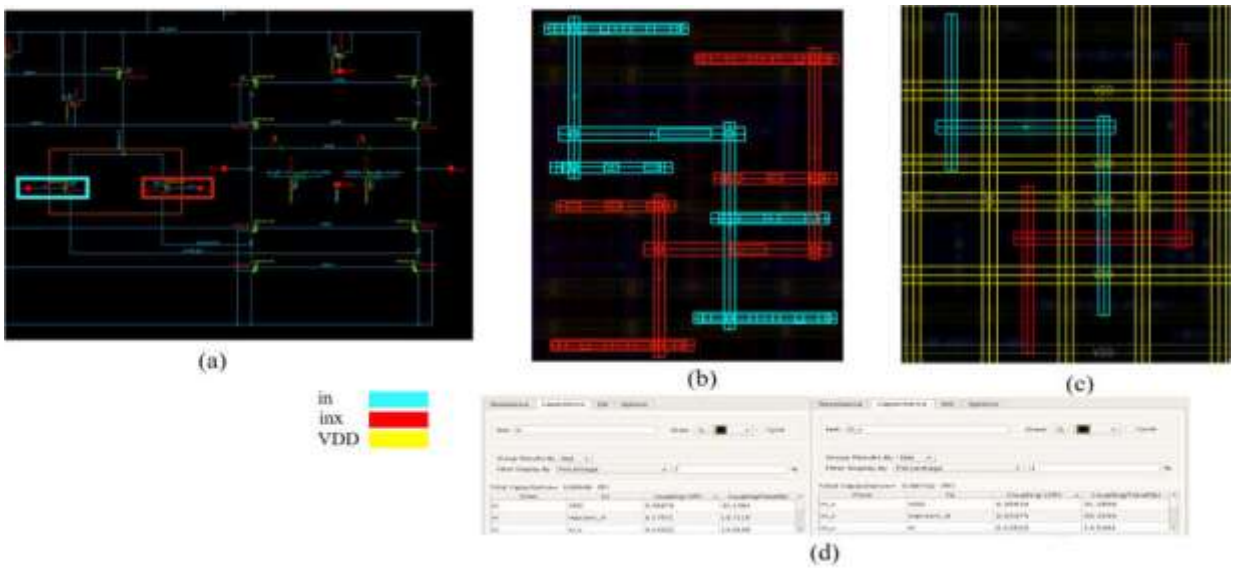


Figure 3.13 (a) in and inx signal in schematic (b) in and inx signal in layout (c) in and inx shielding with vdd (d) Capacitance report

Table 3.6 Metal shielding of signal in and inx

	Min width (μm)	Real width (μm)	Shielding by	Width of shield	Shielding spacing
M4	0.04	0.06	Vdd	0.08	0.1
M3	0.032	0.048	Vdd	0.064	0.112

Secondly, regarding the signals outn (orange) and outp (green) they are also routed to ensure the closest possible matching of capacitance and resistance, illustrated in Figure 3.14 and 3.15. They are shielded by vdd_gated, vdd and vss since the signals lie between the P-region and N-region. Additionally, the signal vdd_gated is derived from the main VDD supply through a control switch. Specifically, VDD passes through a power gating switch, and the output of this switch becomes vdd_gated, which is then used to power the entire circuit. This mechanism allows for controlled power delivery and can help reduce leakage or enable power-down modes when necessary. Therefore, we leverage the power and ground distribution regions for effective shielding.

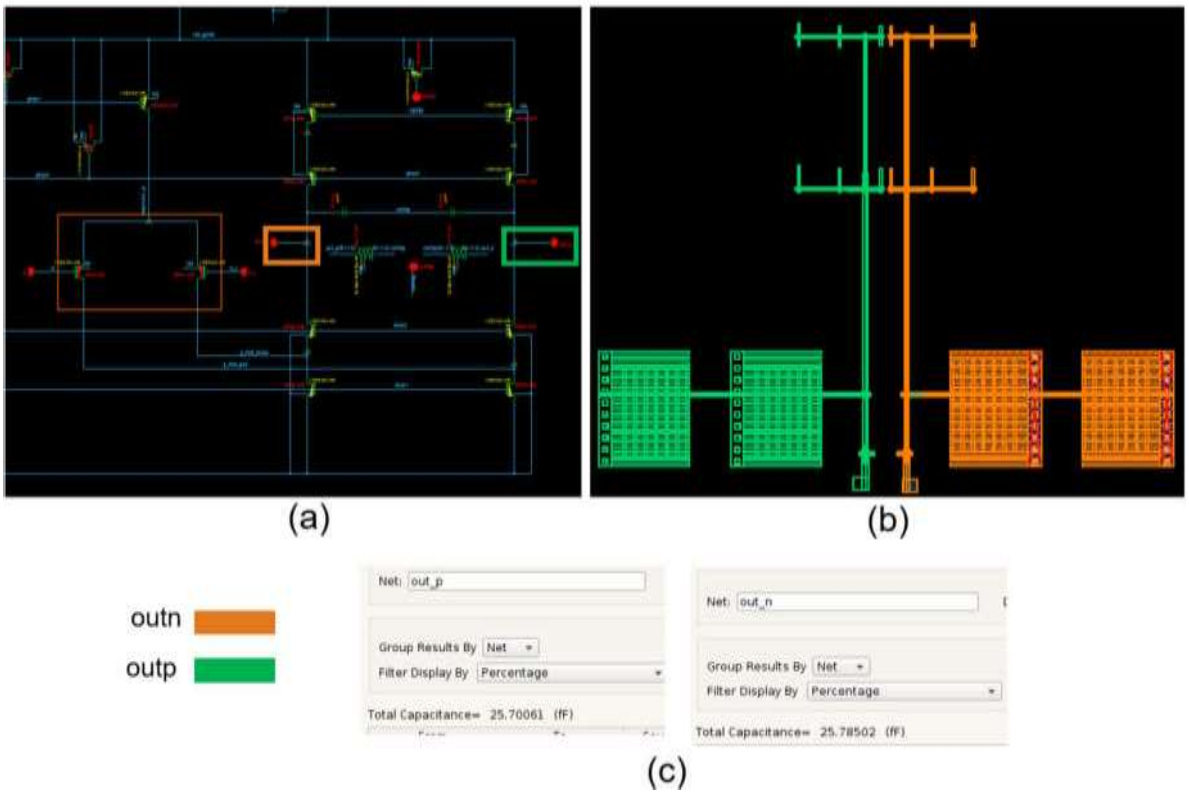


Figure 3.14 (a) Signal outp & outn (b) outp and outn routing (c) Capacitance report

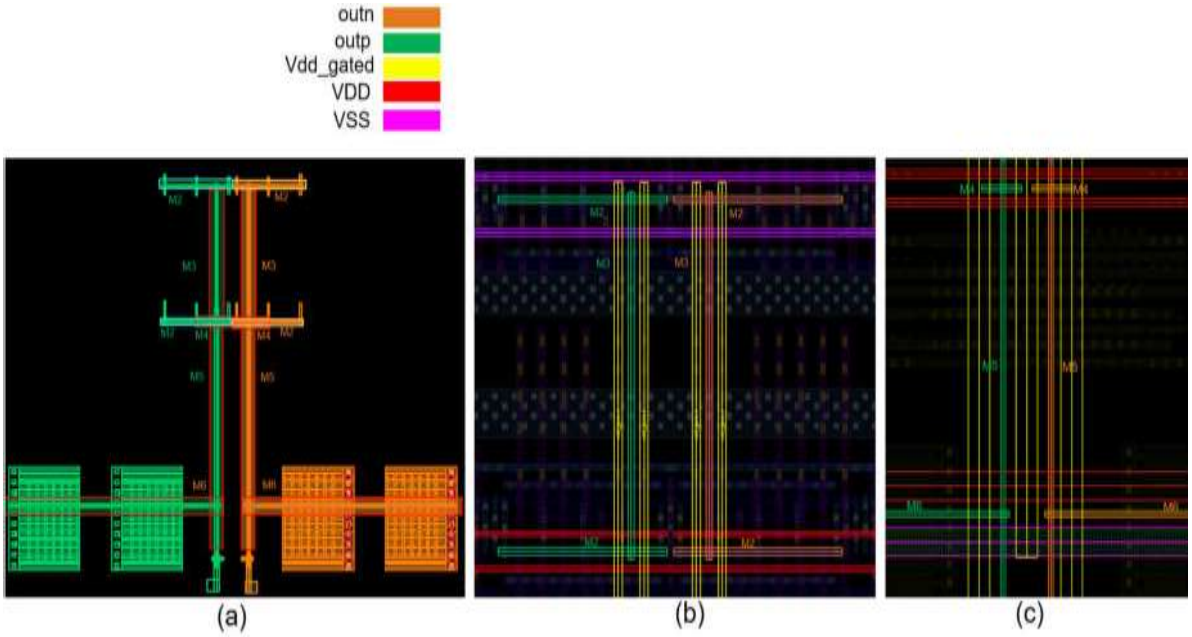


Figure 3.15 (a) outp and outn routing (b) Shielding M2 & M3 (c) Shielding M4 & M5 & M6

Table 3.7 Metal shielding of signal outp and outn

	Min width (μm)	Real width (μm)	Shielding by	Width of shield
M2	0.032	0.048	Vdd/Vss	0.032
M3	0.032	0.048	Vdd_gated	0.064
M4	0.04	0.06	Vdd	0.08
M5	0.04	0.06	Vdd_gated	0.28
M6	0.04	0.06	Vdd/Vss	0.27

In addition to primary signal signals such as in and inx, outp and outn, other critical signals within folded cascode block such as: P_fold_plus and P_fold_minus, net29 and net30 also require careful matching in terms of parasitic capacitance and resistance, illustrating in Figure 3.16, 3.17

Maintaining symmetry and matching for these internal signals is essential to ensure the proper functionality and performance of the folded cascode structure, especially in high-precision analog applications.

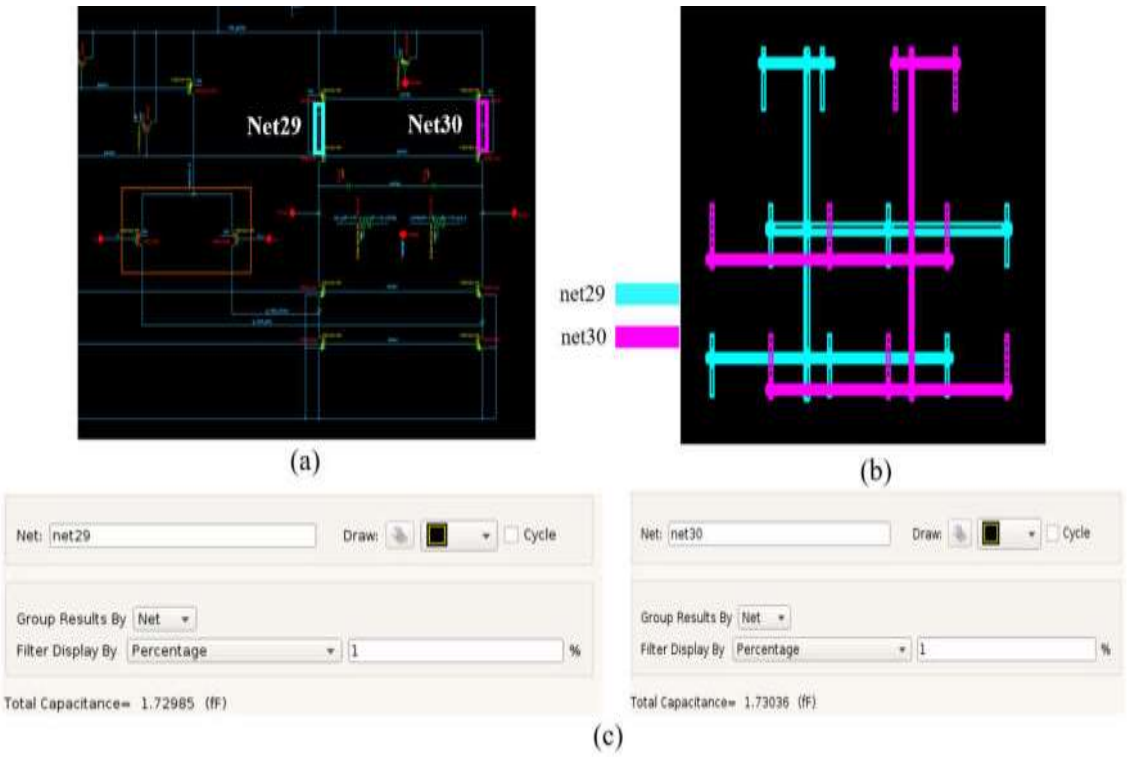


Figure 3.16 (a) net29 and net30 in schematic (b) net29 and net30 routing (c) Capacitance report

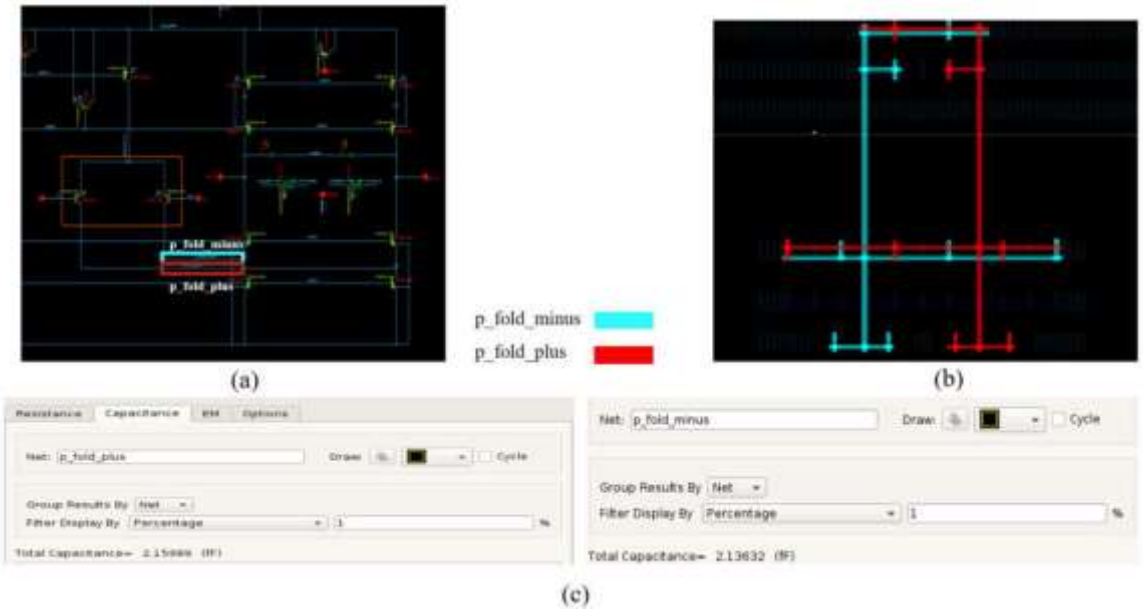


Figure 3.17 (a) p_fold_minus and p_fold_plus in schematic (b) p_fold_minus and p_fold_plus routing (c) Capacitance report

According to the Capacitance Report, the difference in parasitic capacitance between the matched signal pairs is within 0.0x fF, which is negligibly small.

This result confirms that the signals are well matched in terms of capacitance, ensuring balanced performance and minimizing mismatch-induced errors in the analog domain.

3.2.3 Bias Current Block

Based on the matching characteristics of current mirror, the circuit of Bias Current is divided into multiple blocks with two main type of blocks: current mirror and current source.

3.2.3.1 Current Mirror

a. Floorplan

In the biasing circuit, current mirror structures play a critical role in generating supply-independent currents, which are essential for establishing a stable bias voltage for the folded cascode core.

Therefore, in the physical layout, special care must be taken to protect these current mirrors by applying appropriate layout techniques and ensuring full compliance with the requirements listed in Table 3.8.

Table 3.8 Floorplan requirements for current mirror

Num	Requirements	Yes/No
1	Current mirror pair must be matching	Yes
2	Matching pair must have dummy at both sides	Yes
3	Each matching pair must be placed in separated guard-ring	Yes

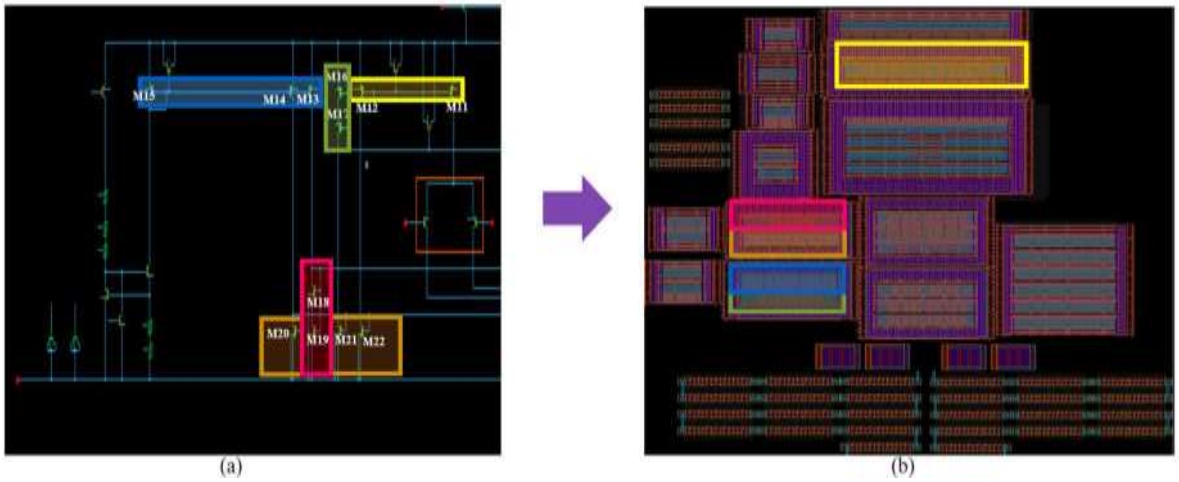


Figure 3.18 (a) Current mirror schematic (b) Current mirror placement

The figure illustrates the schematic and layout placement of current mirrors. To reduce IR drop and improve performance, current mirrors are positioned close to the blocks they bias. The yellow block biases the input differential pair below it. The orange (M20–M22) and pink (M18–M19) blocks bias NMOS devices in the folded cascode, while the blue (M13–M15) and green (M16–M17) blocks are located near the NMOS transistors they support.

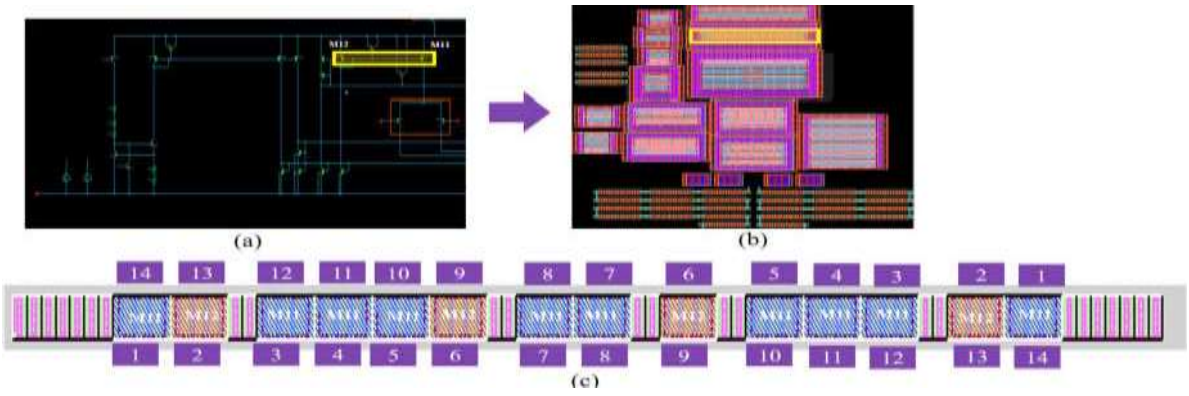


Figure 3.19 (a) Current Mirror Schematic (b) Current Mirror of input pair layout (c) Current Mirror of input pair arrangement

Table 3.9 Size of M11 and M12

	M11	M12
Devices	10	4
Stack of each device	4	4

To ensure accurate current mirroring, the current mirror devices must be carefully matched in layout to reduce mismatch caused by process variations during fabrication. Proper matching significantly improves current copying accuracy, which is critical for analog performance. In this case, M11 consists of 10 devices and M12 consists of 4 devices, with each devices stacked into 4 units as shown in table 3.9. Since the size ratio of M11 to M12 is 10:4, the impact of process variation will also scale proportionally.

The placement shown in Figure 3.19 (c) uses an interleaving technique, which satisfies this ratio and helps balance systematic gradient effects

Similarly, other current mirror pairs are arranged following the same matching principles, as shown in the figures below

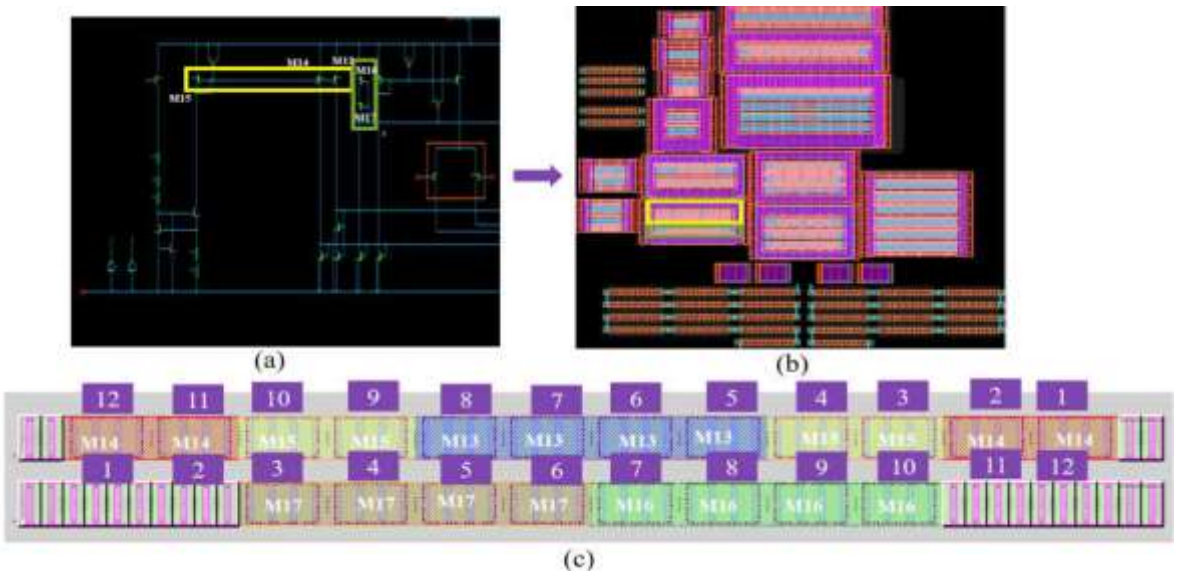


Figure 3.20 (a) Current Mirror Schematic (b) Current Mirror layout (c) Current Mirror arrangement

In this case, M14 and M13 mirror the current from M15, so M15 is placed at the center of the layout. This central placement ensures that the current copied from M15 to M14 and from M15 to M13 experiences symmetrical routing conditions, minimizing mismatches caused by gradient effects and layout asymmetry.

b. Signal routing

In addition to floorplanning requirements, it is also essential to consider the routing of critical bias signals to ensure optimal performance in the biasing circuit. These key signals include: pbias0, pbias1, pbias2, nbias1, nbias2. In the physical design, the requirements listed in table 3.10 must be followed.

Table 3.10 Signal routing requirements

Num	Requirements	Yes/No
1	Routing from the current mirror to the objects it biases should be as short as possible	Yes
2	Shielding Bias net (Pbias0, Pbias1, Pbias2, Nbias1, Nbias2)	Yes
3	Width of critical signals must be passed EM	Yes
4	Current mirror pair must have connection to both ends of Poly gates	Yes

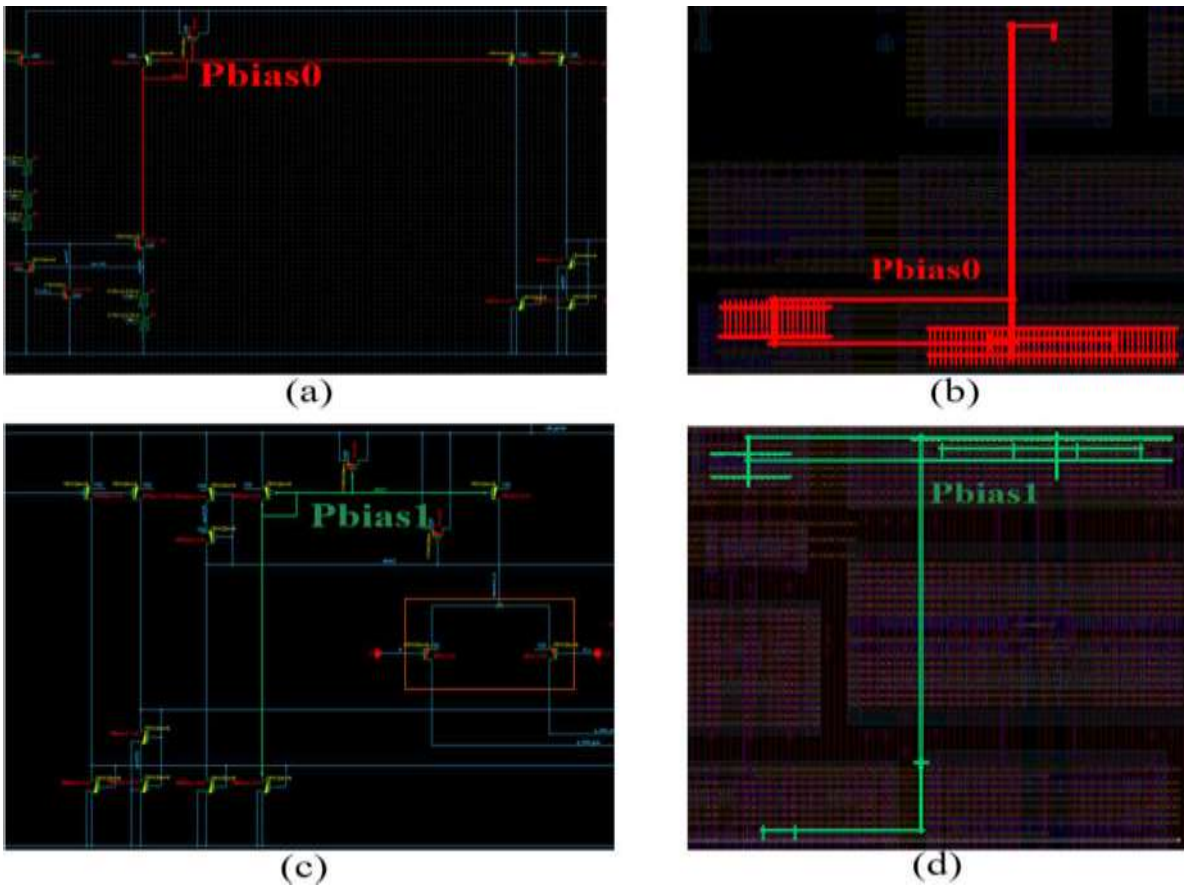


Figure 3.21 (a) Pbias0 signal in schematic (b) Pbias0 signal in layout a) Pbias1 signal in schematic (b) Pbias1 signal in layout

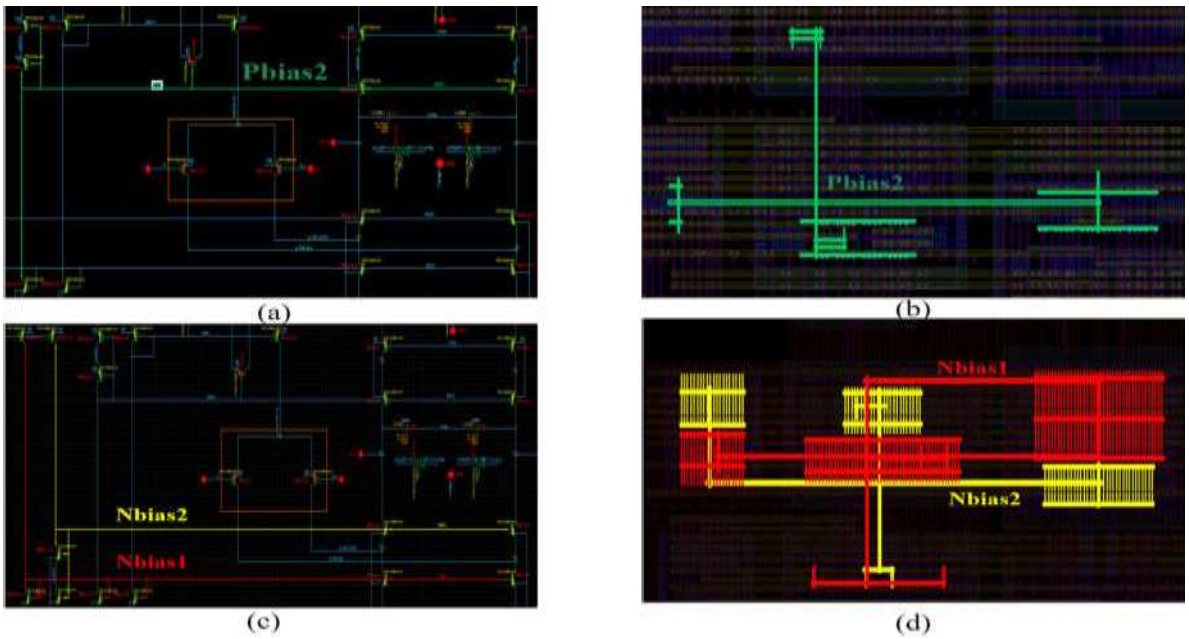


Figure 3.22 (a) Pbias2 signal in schematic (b) Pbias2 signal in layout a) Nbias1 and Nbias2 signal in schematic (b) Nbias1 and Nbias2 signal in layout

To ensure the stability and integrity of bias signals within the bias current circuit, shielding techniques are applied to critical bias nets, illustrated in figure 3.23 & 3.24 & 3.25 & 3.26 & 3.27. These signals are typically high-impedance and highly sensitive to noise, particularly from nearby switching signals or power distribution networks. By applying appropriate shielding, the design can minimize interference, suppress parasitic coupling, and enhance the reliability and precision of the bias network. In this layout, the shielding lines Vdd, Vss, or Vdd_gated are selected based on the functional domain through which the signal passes.

Table 3.11 Metal shielding of signal Pbias0

	Min width (μm)	Real width (μm)	Shielding by	Width of shield
M2	0.032	0.048	Vdd/Vdd_gated	0.032
M3	0.032	0.048	Vss/Vdd_gated	0.064
M4	0.04	0.06	Vdd_gated	0.08

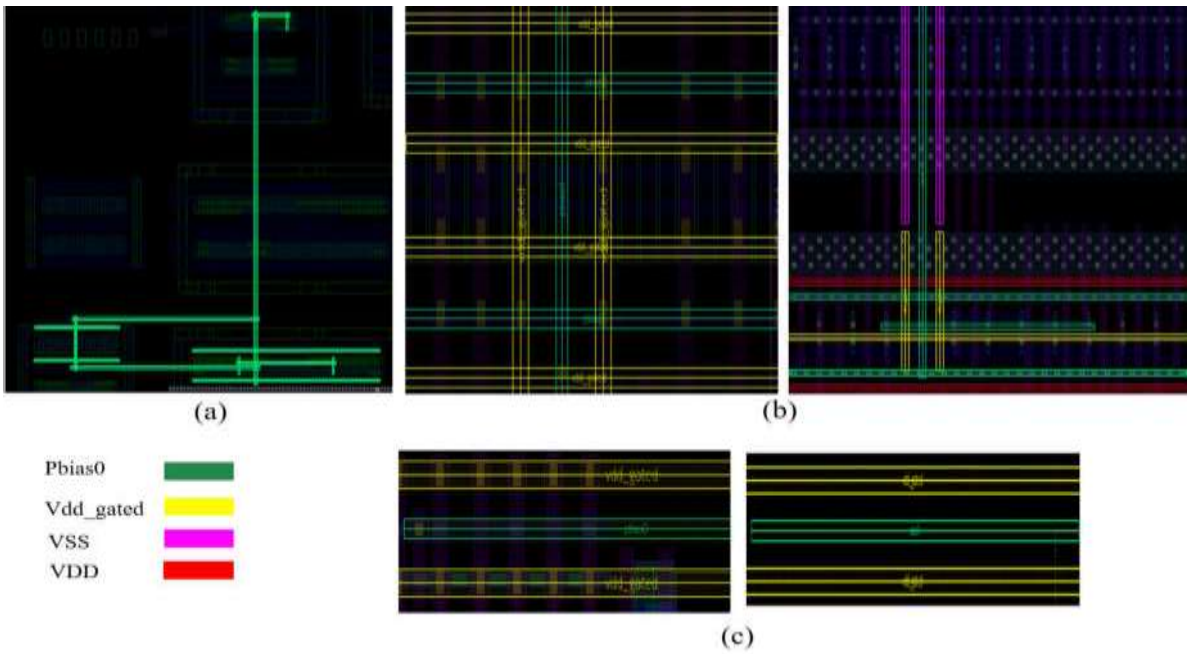


Figure 3.23 (a) Pbias0 signal (b) Shielding M2&M3 (c) Shielding M4

Table 3.12 Metal shielding of Pbias1 signal

	Min width (μm)	Real width (μm)	Shielding by	Width of shield
M2	0.032	0.048	Vss/Vdd/Vdd_gated	0.048
M3	0.032	0.048	Vss/Vdd_gated	0.064
M4	0.04	0.06	Vdd_gated	0.08
M5	0.04	0.06	Vdd	0.28

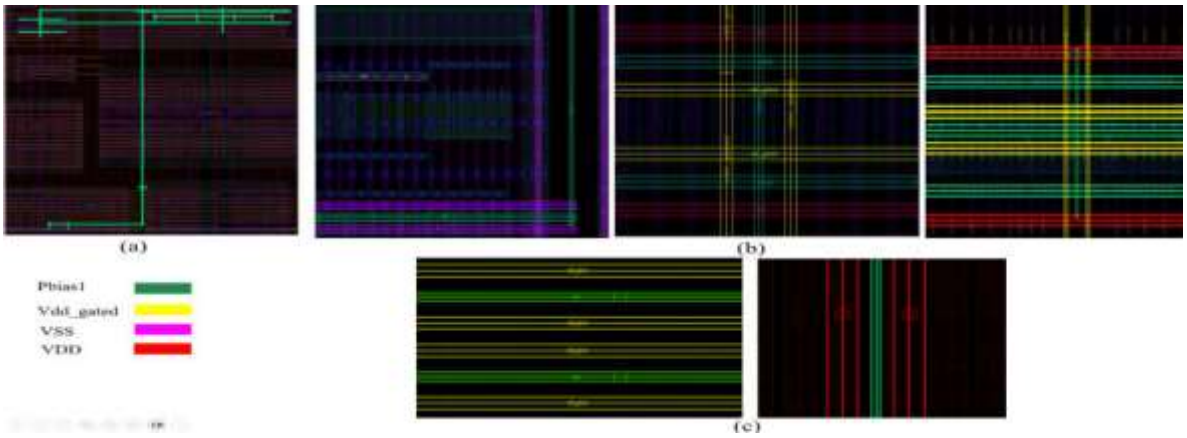


Figure 3.24 (a) Pbias1 signal (b) Shielding M2&M3 (c) Shielding M4&M5

Table 3.13 Metal shielding of signal Pbias2

	Min width (μm)	Real width (μm)	Shielding by	Width of shield
M2	0.032	0.048	vdd_gated/ Vdd	0.048
M3	0.032	0.048	Vdd_gated/Vss	0.064
M4	0.04	0.06	Vdd_gated	0.08

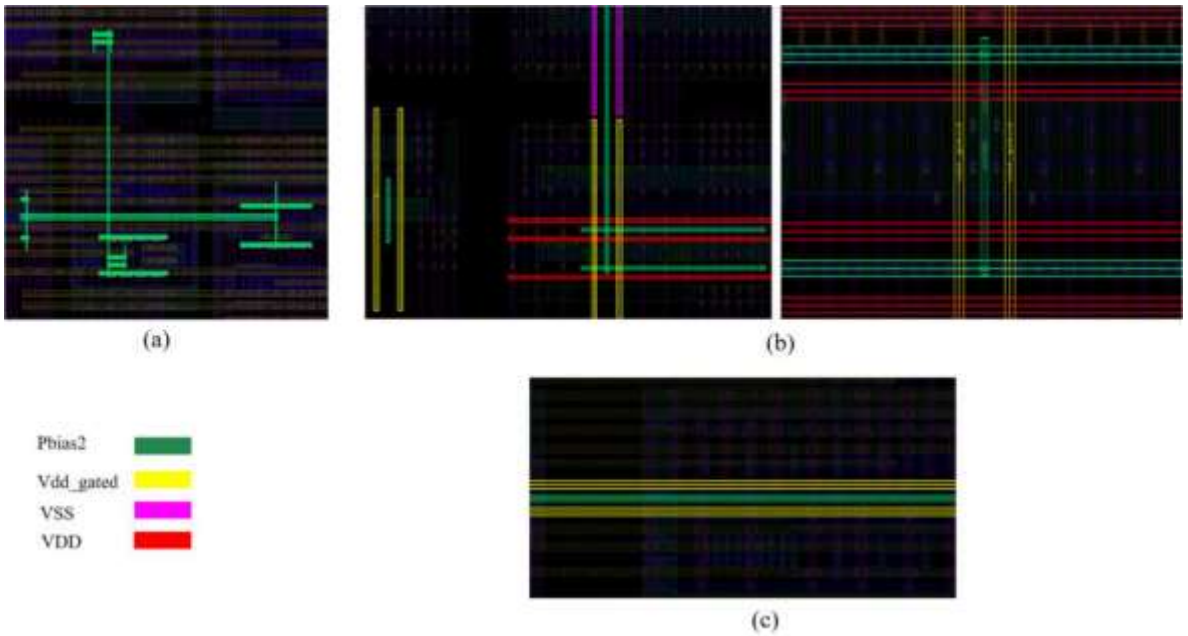


Figure 3.25 (a) Pbias2 signal (b) Shielding M2&M3 (c) Shielding M4

Table 3.14 Metal shielding of signal Nbias1

	Min width (μm)	Real width (μm)	Shielding by	Width of shield
M2	0.032	0.048	Vss	0.048
M3	0.032	0.048	Vdd_gated/Vss	0.064
M4	0.04	0.06	Vss	0.08

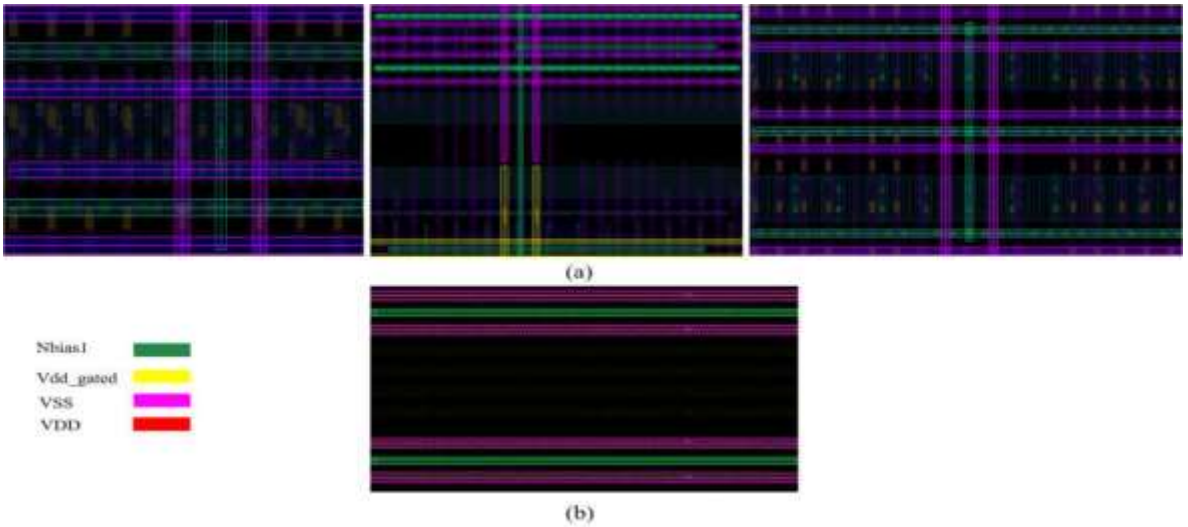


Figure 3.26 (a) Shielding M2&M3 of signal Nbias1 (b) Shielding M4 of signal Nbias1

Table 3.15 Metal shielding of signal Nbias2

	Min width (μm)	Real width (μm)	Shielding by	Width of shield
M2	0.032	0.048	Vss	0.048
M3	0.032	0.048	Vss/Vdd_gated	0.064
M4	0.04	0.06	Vss	0.08

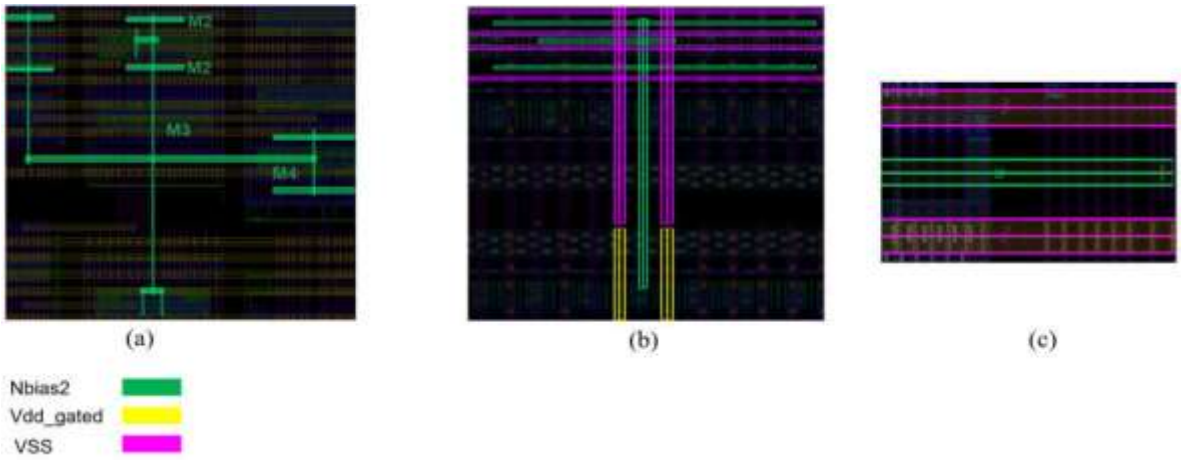


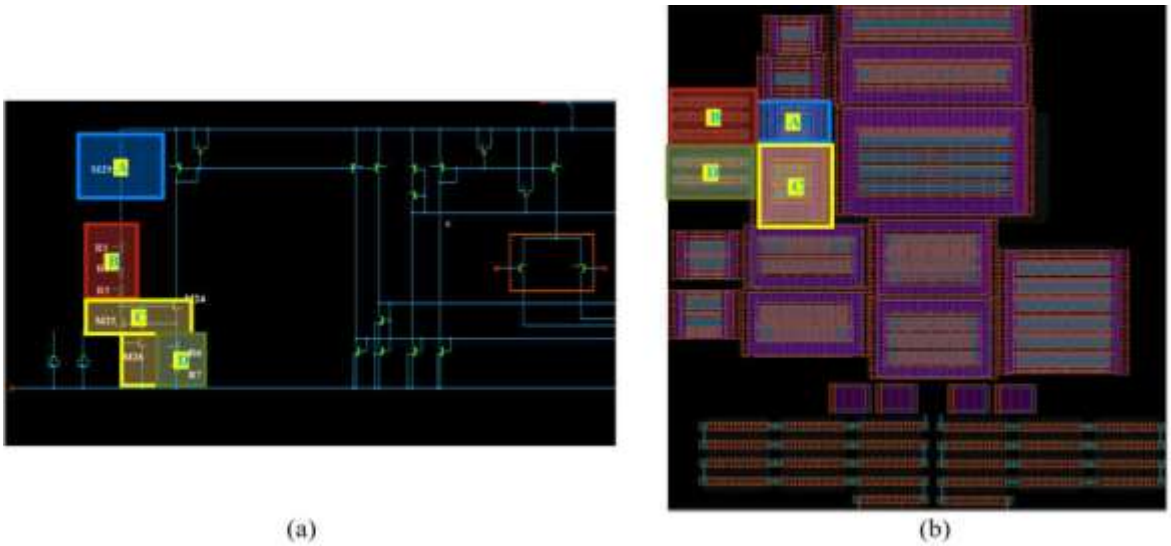
Figure 3.27 (a) Nbias2 signal (b) Shielding M2&M3 (c) Shielding M4

3.2.3.2 Current Source

a. Floorplan

Table 3.16 Floorplan requirements for current source

Num	Requirements	Yes/No
1	M24 and M25 pair must be same OD	Yes
2	M24 and M25 must place in a guardring	Yes
3	Add dummies at both side for each device of current source	Yes
4	Using two-sided bulk for non-matching devices	Yes



(a) (b)

Figure 3.28 (a) Current Source schematic (b) Current Source floorplan

The floorplanning of the current source block follows several key layout requirements, each with a specific design rationale:

- M24 and M25 must have the same OD (diffusion area). This requirement is to avoid mismatch during fabrication and ensure consistent current mirroring performance.
- M24 and M25 must be placed inside a guard ring: The guard ring is used to isolate the devices from substrate noise, protecting the biasing accuracy.
- Dummy transistors must be added on both sides of each device: This helps to reduce layout-dependent effects such as STI stress and well proximity, which can degrade device matching.
- Two-sided bulk connection is used for non-matching devices: This approach allows for area saving and shorter routing paths, contributing to a more compact and efficient layout.

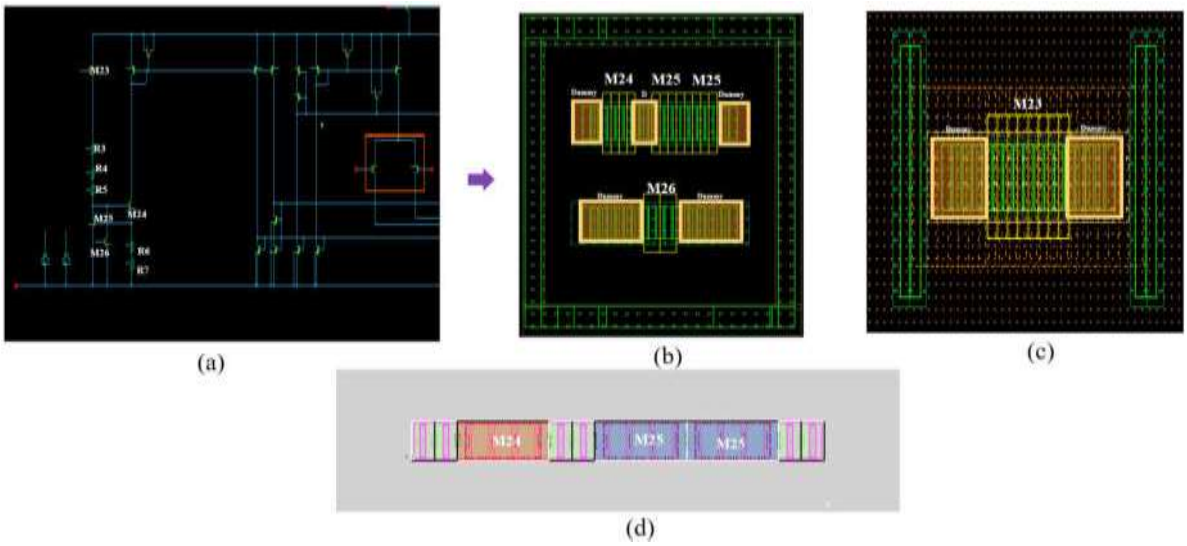


Figure 3.29 (a) Current Source schematic (b) M24, M25, M26's Guardring (c) M23's two-sided bulk (d) M24, M25 arrangement

b. Signal routing requirements

Regarding the signal routing requirements of the current source block, there are no critical constraints to be enforced. The primary objective is to keep the routing paths as short as possible in order to minimize IR drop along the metal lines and maintain bias stability.

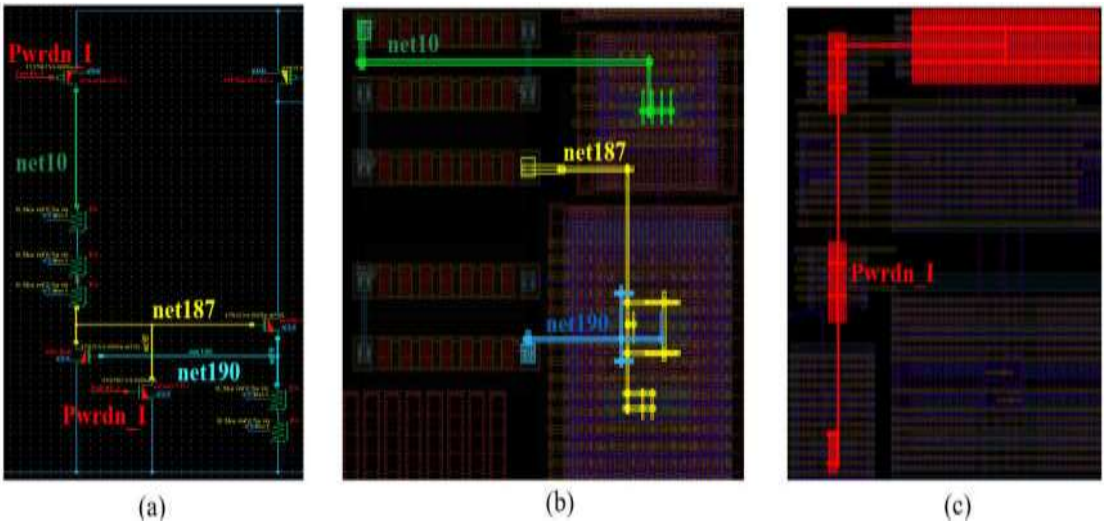


Figure 3.30 (a) Current source schematic (b) Net10, Net187, Net190 routing (c) Pwrdn_I routing

3.2.4 Electromigration (EM) Evaluation

The movement of atoms caused by the flow of electricity through a substance is known as electromigration. The heat dissipated within the material will repeatedly break atoms from the structure and transport them if the current density is high enough.

To avoid EM issues during physical design, several equations based on required technology will be used to calculate metal width and to be aware of this problem. According to the DRM The DC current of a metal can maintain can be calculated as:

$$I_{dc} = I_{dc}' \times F(T) \times F(EOL_{actual}) \times F(duty) \quad (3.2)$$

Where I_{dco} is the DC current limit at $105°C$ for an 87600 hours product lifetime at CDF (cumulative distribution function) = 1E-1%, F(T) is a function of F with respect to temperature (in our design the worst case $105°C$ is used for simulation), $F(EOL_{actual})$ is the design sign-off time of chip, in this case, is 10 years (means 87600 hours).

From that we can calculate the metal width required for design as following table

Table 3.17 EM Evaluation

EM evaluation								
Signal	**Average DC current (I mA) at $105°C$**	**Metal Width**						**PASS EM (YES/NO)**
		M1	**M2**	**M3**	**M4**	**M5**	**M6**	
In	0.05	0.032	0.048	0.048	0.06			YES
Inx	0.05	0.032	0.048	0.048	0.06			YES
Outp	0.04	0.032	0.048	0.048	0.06	0.06	0.06	YES
Outn	0.04	0.032	0.048	0.048	0.06	0.06	0.06	YES
Mpcssrc_d	0.1	0.032	0.048	0.048				YES
P_fold_plus	0.05	0.032	0.048	0.048				YES
P_fold_minus	0.05	0.032	0.048	0.048				YES
Pbias0	0.04	0.032	0.048	0.048	0.06			YES
Pbias1	0.04	0.032	0.048	0.048	0.06	0.06		YES
Pbias2	0.04	0.032	0.048	0.048	0.06			YES
Nbias1	0.04	0.032	0.048	0.048	0.06			YES
Nbias2	0.04	0.032	0.048	0.048	0.06			YES

3.3 Chapter Conclusion:

In this chapter, the operating principles of each block within the Duty Cycle Detector (DCD) circuit—namely the Folded Cascode, Current Mirror, and Current

Source—have been thoroughly presented. The chapter also provides an in-depth discussion of the physical design for each block, applying layout techniques previously introduced to meet design requirements and to maximize the performance and stability of the circuit.

This chapter establishes a solid foundation for the results and analyses presented in the following chapter.

CHAPTER 4: EXPERIMENTAL RESULTS AND EVALUATION OF THE HIGH-SPEED DUTY CYCLE ADJUSTMENT

This chapter focuses on presenting the experimental results and evaluation of the high-speed duty cycle detector. It is crucial to assess its performance and effectiveness through practical experiments by stimulating the Folded Cascode and Bias Current at different PVT corners, as shown in table 4.1. In this chapter, we discuss the layout design, analyze the results, and draw conclusions based on the evaluation. Furthermore, we analyze the results obtained from the experiments. This includes the pre-layout simulation results, post-layout simulation results, and a comprehensive analysis of the obtained data.

Table 4.1 PVT Corners

Process	**Res/Cap**	**nMOS/pMOS**	**Temperature (°C)**	**VDD (V)**	**VCCIO (V)**	**Extraction type**
TT	T/T	T/T	25	0.85	0.45	typical
SS	L/L	S/S	-40 125	0.765 0.935	0.414 0.473	SigRCmax SigRCmin
SF		S/F				
FS	H/H	F/S				
FF		F/F				

To be more specific, the process is consisting of 3 kinds of processes: TT (Typical-Typical), FF (Fast-Fast), and SS (Slow-Slow). It indicates the strength of NMOS and PMOS devices, respectively. The strength is related to the mobility of electrons in these devices. In terms of voltage, VCCIO would vary according to the process and temperature with +8%/-5% and VDD would vary with +/-10%. Next, the range of temperature is from -40^0C to 125^0C with the typical value of temperature being 25^0C. Finally, the extraction type of resistance and capacitance on all nets is based on the PVT. For process FF, the value of resistance and capacitance are the best, which means these values are minimal. In contrast, for process SS, these values are the worst or largest.

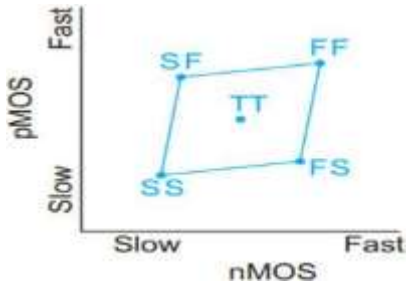


Figure 4.1 Process corners for CMOS devices

4.1 Simulation results of Prelayout and Postlayout

4.1.1 DCOP Analysis

The results of the DCOP analysis are shown in table 4.2 & 4.3 & 4.4 & 4.5 & 4.6 & 4.7 & 4.8. In this case, only the maximum and minimum values are illustrated since it is monotonous to observe the value of all corners.

4.1.1.1 Current source

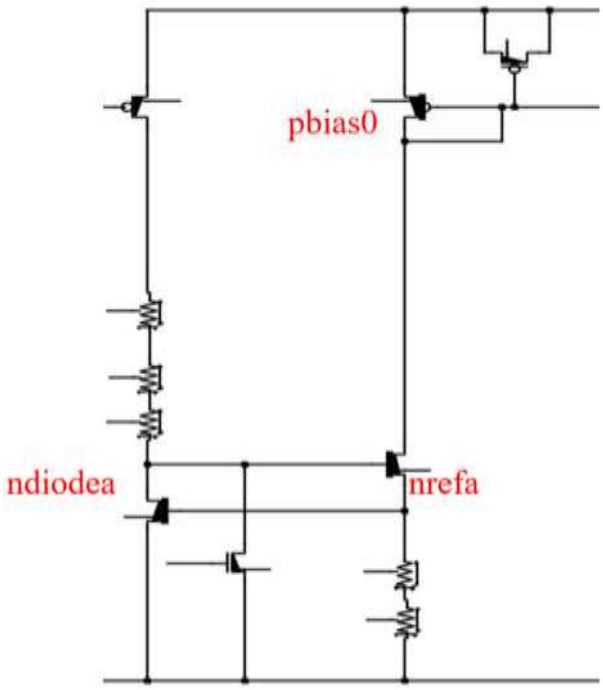


Figure 4.2 Current source schematic

Table 4.2 The DCOP of analog devices of pre-layout

Transistor	$V_{OD} > -0.1V$		$V_{\text{margin}} > 0V$		**Current** (A)	
	Min	**Max**	**Min**	**Max**	**Min**	**Max**
ndiodea	-0.007	0.108	0.042	0.615	1.78	23.1
nrefa	0.105	0.184	0.172	0.052	33.12	51.48
pbias0	0.056	0.113	0.285	0.408	33.12	52.88

Table 4.3 The DCOP of analog devices of post-layout

Transistor	$V_{OD} > -0.1V$		$V_{\text{margin}} > 0V$		**Current** (A)	
	Min	**Max**	**Min**	**Max**	**Min**	**Max**
ndiodea	-0.015	0.108	0.416	0.625	1.22	21.357
nrefa	0.116	0.192	0.153	0.025	32.203	51.45
pbias0	0.054	0.11	0.136	0.339	32.21	52.73

Comment: From the results shown in Tables 4.2 and 4.3, it can be observed that the values of Vod, Vmargin, and current differ between the pre-layout and post-layout simulations. This difference is mainly due to the increase in parasitic resistance (R) and capacitance (C) within the devices after layout. Additionally, the MOSFET models used in layout and schematic simulations are not identical, which also contributes to the variation. However, the differences are relatively small—on the order of a few millivolts and microamperes—so they are considered acceptable. Most importantly, the overall circuit specifications are still met, and the design remains valid.

4.1.1.2 Current mirror

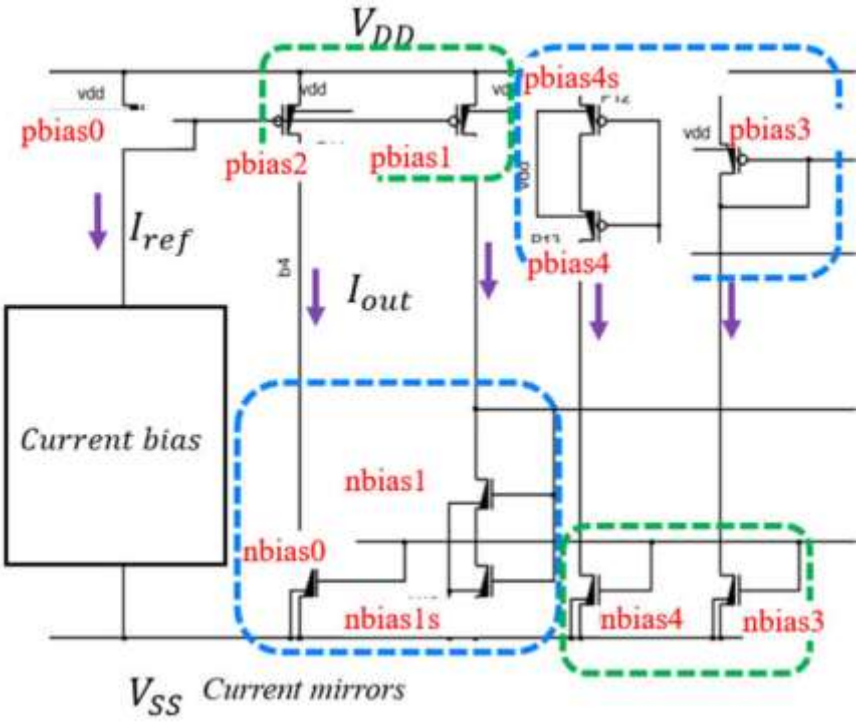


Figure 4.3 Current Mirror Schematic

Table 4.4 The DCOP of analog devices of pre-layout

Transistor	$V_{OD} > -0.1V$		$V_{\text{margin}} > 0V$		**Current** (A)	
	Min	**Max**	**Min**	**Max**	**Min**	**Max**
nbias0	0.037	0.108	0.128	0.238	33.064	55.148
nbias1, nbias1s	0.146	0.217	0.216	0.315	32.44	54.24
pbias4, pbias4s	0.132	0.185	0.206	0.336	32.464	56.6
pbias3	0.059	0.116	0.150	0.287	32.86	56.82
nbias3	0.041	0.114	0.160	0.412	31.7	56.581
nbias4	0.0412	0.114	0.107	0.338	32.565	57.77
pbias1	0.053	0.109	0.117	0.321	31.079	53.54
pbias2	0.053	0.109	0.211	0.445	33.277	56.376

Table 4.5 The DCOP of analog devices of post-layout

Transistor	$V_{OD} > -0.1V$		$V_{\text{margin}} > 0V$		Current (A)	
	Min	Max	Min	Max	Min	Max
nbias0	0.05	0.122	0.127	0.237	33.276	56.375
nbias1, nbias1s	0.15	0.222	0.212	0.308	31.079	53.539
pbias4, pbias4s	0.13	0.182	0.206	0.336	32.565	57.77
pbias3	0.054	0.111	0.148	0.286	31.7	56.21
nbias3	0.041	0.114	0.160	0.412	31.7	56.581
nbias4	0.0412	0.114	0.107	0.338	32.565	57.77
pbias1	0.053	0.109	0.117	0.321	31.079	53.54
pbias2	0.053	0.109	0.211	0.445	33.277	56.376

Comment: The same reason as above, that causes that he results from post-layout and pre-layout are a bit different, but the difference is acceptable because it still meets the required specifications.

4.1.1.3 Folded Cascode

Here, Matching pairs are: (mpin & mpinx), (mp1p & mp1n), (mp2p & mp2n), (mn2p & mn2n), (mn1p & mn1n)

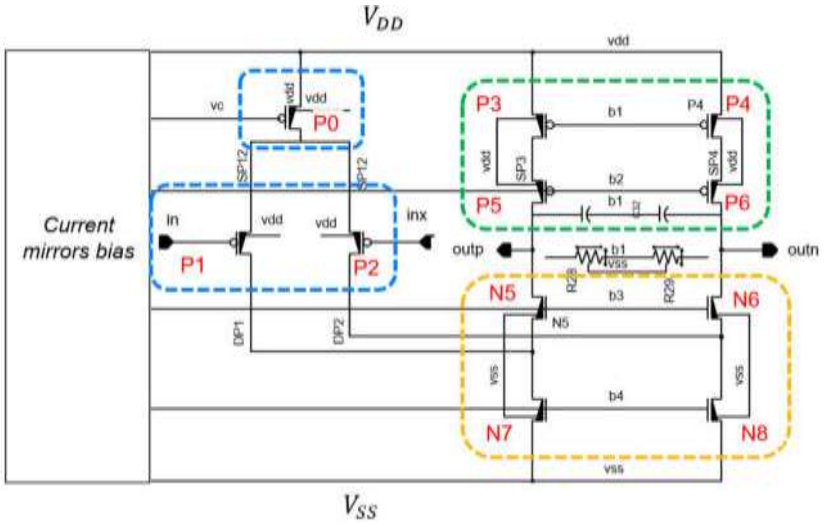


Figure 4.4 Folded Cascode Schematic

Table 4.6 The DCOP of analog devices of pre-layout

Transistor	$V_{OD} > -0.1V$		$V_{\text{margin}} > 0V$		**Current** (A)	
	Min	**Max**	**Min**	**Max**	**Min**	**Max**
mpcssrc	0.059	0.116	0.005	0.256	75.98	143.7
mpin, mpinx	0.059	0.138	0.192	0.377	37.988	73.44
mp1p, mp1n	-0.001	0.065	0.083	0.05	29.88	47.71
mp2p, mp2n	0.052	0.109	0.011	0.171	29.88	47.84
mn2p, mn2n	0.027	0.099	0.127	0.372	29.88	47.6
mn1p, mn1n	0.037	0.108	0.09	0.019	68.84	120.7

Table 4.7 The DCOP of analog devices of pre-layout

Transistor	$V_{OD} > -0.1V$		$V_{\text{margin}} > 0V$		**Current** (A)	
	Min	**Max**	**Min**	**Max**	**Min**	**Max**
mpcssrc	0.056	0.112	-0.002	0.243	72.856	141.895
mpin	0.053	0.133	0.190	0.376	36.429	72.317
mpinx	0.053	0.133	0.189	0.376	36.426	72.309
mp1p	-0.004	0.061	0.081	0.049	28.587	47.012
mp1n	-0.005	0.06	0.081	0.049	28.59	47.016
mp2p	0.047	0.103	0.006	0.168	28.597	47.14
mp2n	0.047	0.104	0.006	0.167	28.597	47.139
mn2p	0.030	0.102	0.114	0.353	28.589	47.048
mn2n	0.030	0.103	0.114	0.353	28.593	47.051
mn1p	0.041	0.113	0.079	0.008	65.754	118.913
mn1n	0.041	0.114	0.079	0.009	65.759	118.926

Comment: The same reason as above, that causes that he results from post-layout and pre-layout are a bit different, but the difference is acceptable. To more specific, post-layout of signal mpcssrc fails Vmargin, but can be waived, because the failing corner is one of the worst cases (res_high, cap_high, vdd_min=0.75vdd), the rest of corner is still passed and still have enough current to bias input diff pair, so still meet specifications

Regarding the matching pairs, the values of ɾ, Vmargin, and current are approximately equal. This indicates that the matching between these pairs has been successfully achieved.

In conclusion, all matching pairs are well-matched, and the functionality of the folded cascode circuit is preserved as intended.

4.1.2 DC gain and stability measurement results

Table 4.8 Gain and Stability Results of the Folded Cascode Block

Parameter	Specification		Pre-layout		Post-layout		Unit	Judgment
	Min	Max	Min	Max	Min	Max		
Supply Voltage	0.765	0.935	0.765	0.935	0.765	0.935	V	
DC Gain	16	-	17.69	24.86	17.63	24.58	dB	PASS
Gain margin	20	-	29.02	31.89	27.47	28.45	dB	PASS
Phase margin	50	-	74.6	92.54	80.5	96.8	Degree	PASS

Comment: All parameters meet the initial design specifications. Both phase margin and gain margin satisfy the required conditions, confirming that the system is stable. The low-frequency gain (DC gain) also meets the targeted value.

Although the post-layout results show slight deviations compared to the pre-layout simulation due to parasitic effects introduced by the physical layout, these variations are within acceptable limits and do not affect the overall functionality.

Therefore, it can be concluded that the Folded Cascode block is well-suited for integration with subsequent stages in the DCD circuit.

4.1.3 Transient analysis result

Table 4.9 Vcm and Power Measurement Results of the Folded Cascode Circuit

Parameter	Specification		Pre-layout		Post-layout		Unit	Judgment
	Min	Max	Min	Max	Min	Max		
Supply Voltage	0.765	0.935	0.765	0.935	0.765	0.935	V	
Vcm in mission mode	250	-	390.3	666.4	387.9	663.1	mV	PASS
Voutp in mission mode	-	-	390.3	666.4	388.1	663.1	mV	
Voutn in mission mode	-	-	390.3	666.4	387.7	663.1	mV	
Power in mission mode	-	-	0.5474	0.3	0.29	0.5414	mV	
Power in power down mode	-	-	0.063	0.000012	0.016	0.023	mV	

Comment: All parameters meet the initial design specifications. The Vcm is high, power consumption is moderate, and in the off state, leakage current is minimal, indicating that the design meets the required criteria. The post-layout results show slight deviations compared to the pre-layout data due to parasitic effects, but the differences are within acceptable limits. Additionally, Voutp and Voutn in mission mode are nearly identical, which confirms the balanced operation of the folded cascode output stage.

4.2 Physical Verification report

To analyze how good our design after Layout progresses, the post-layout simulation must be involved. And if we want the result of post-layout simulation to be most accurate, the design must pass LVS. So here is the detailed table to summarize and report the status of our physical design.

Table 4.10 Physical verification report

Items	**Mode**	**Status**
LVS	Internal	Pass
LVS	Tape-out	Pass
DRC	Internal	Clean
DRC	Tape-out	Clean
SDL		Pass
EMIR		Just hand calculation for EM

4.3 Chapter Conclusion:

In this chapter, the measurement results of both the schematic-level design and physical layout of the Bias Current and Folded Cascode circuits within the DCD system have been thoroughly presented.

The circuit is fully capable of amplifying the differential signal between the positive and negative input terminals, and its output can be fed into the Strong-Arm Latch block to effectively fulfill the overall function of the Duty Cycle Detector (DCD).

CONCLUSION AND FUTURE WORK

1. Conclusion

Through the implementation of this project, I have studied and grasped the fundamental theories of semiconductors, CMOS technology, common effects, and layout techniques used in physical design. I successfully completed the physical design of folded cascode and Bias current in DCD circuit. In the layout process, various techniques were applied, including device placement strategies, guard rings, shielding, and dummy devices, among others. The circuit was simulated, and although there were some deviations between the post-layout and pre-layout results, the differences remained within the acceptable error range defined by the project requirements.

2. Future Work

Due to time constraints, the current scope of the project has been limited to the layout design of the Folded Cascode and Bias Current blocks, along with corresponding pre-layout and post-layout simulations. However, other functional blocks within the DCD circuit have not yet been designed or implemented, which restricts a comprehensive evaluation of overall system performance, area usage, and stability. This, in turn, affects the integration capability and completeness of the system.

In future work, to enhance the quality and practical applicability of the design, efforts will be focused on completing the remaining functional blocks of the DCD circuit. This includes both schematic design and physical layout, followed by full-chip post-layout simulations to verify the performance of the entire system.

To minimize discrepancies between pre-layout and post-layout results, i plan to further optimize the layout, with special attention to device placement and signal routing techniques.

These improvements aim to reduce layout parasitics, optimize silicon area, improve matching accuracy, and enhance the overall stability of the Duty Cycle Detector. Ultimately, these enhancements will contribute to better compliance with the stringent requirements of modern electronic systems.

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